2017

Design of a low power 8-bit A/D converter for wireless neural recorder applications

https://hdl.handle.net/2144/23685

Boston University
DESIGN OF A LOW POWER 8-BIT A/D CONVERTER FOR
WIRELESS NEURAL RECORDER APPLICATIONS

by

JIAO YANG
B.E., Southeast University, 2014

Submitted in partial fulfillment of the
requirements for the degree of
Master of Science
2017
Approved by

First Reader

Ronald W. Knepper, Ph.D.
Professor of Electrical and Computer Engineering

Second Reader

Allyn E. Hubbard, Ph.D.
Professor of Electrical and Computer Engineering
Professor of Biomedical Engineering

Third Reader

Mark N. Horenstein, Ph.D.
Professor of Electrical and Computer Engineering
DEDICATION

I would like to dedicate this work to my beloved parents and friends, for their everlasting love, patience and support.
ACKNOWLEDGMENTS

I would like to show my deepest acknowledgement and respect to Professor Ronald W. Knepper, my erudite advisor, who guides me in discovery of VLSI circuit design and helps me get over countless difficulties and challenges during the realization of my thesis.
DESIGN OF A LOW POWER 8-BIT A/D CONVERTER FOR WIRELESS NEURAL RECORDER APPLICATIONS

JIAO YANG

ABSTRACT

Human brain and related topics like neuron spikes and their active potentials have become more and more attractive to people these days, as these issues are extremely helpful for curing many neural injuries and cognitive diseases. One method to discover this field is by designing a chip embedded in brains with probes to actual neurons. It is obvious that batteries are not practical for these applications and thereby RF radiation is used as power sources, revealing that chips should operate under a very low power supply. Since neural signals are analog waveforms, analog-to-digital converter (A/D converter, ADC) is the key component in a neural recorder chip.

This thesis proposes the complete design of a low power 8-bit successive approximation register (SAR) A/D converter for use in a wireless neural recorder chip, realizing the function of digitizing a sampled neural signal with a frequency distribution of 10Hz to 10kHz. A modified energy-saving capacitor array in the SAR structure is provided to help save power dissipation. Therefore, the ADC shall operate within a power budget of 20-μW maximum from a 1-V power source, at a clock frequency of 500kHz corresponding to a conversion rate of 55.5-kS/s. All the circuits are designed and implemented based on the IBM/Global Foundries 8HP 130nm BiCMOS technology. Simulations of schematic and layout versions are done respectively to verify the functionality, linearity and power consumption of the ADC.
Key words: Successive approximation register analog-to-digital converter (SAR-ADC), low power design, energy-saving capacitor array, neural recorder applications
# TABLE OF CONTENTS

DEDICATION .................................................................................................................. iv

ACKNOWLEDGMENTS ............................................................................................... v

ABSTRACT .................................................................................................................... vi

TABLE OF CONTENTS ............................................................................................... viii

LIST OF TABLES ......................................................................................................... x

LIST OF FIGURES ....................................................................................................... xi

CHAPTER 1: BACKGROUND ....................................................................................... 1

1.1 Neural Recorder Chip ......................................................................................... 1

1.2 Requirements for ADC Design in Neural Recorder Chip ................................. 2

1.3 ADC Type Comparison ...................................................................................... 2

CHAPTER 2: CIRCUIT DESIGN ................................................................................... 4

2.1 System Block Diagram ..................................................................................... 4

2.2 Latched Comparator .......................................................................................... 4

2.3 Differential Binary-weighted Capacitor Array ................................................. 7

2.4 Control Logic .................................................................................................... 32

2.5 Other Digital Modules ...................................................................................... 33

CHAPTER 3: ENERGY-EFFICIENCY ALGORITHM .................................................. 36

3.1 Conventional SAR Algorithm .......................................................................... 36

3.2 Capacitor Splitting Technology ....................................................................... 39

viii
CHAPTER 4: LAYOUT IMPLEMENTATION ................................................................. 41
  4.1 Overview ..................................................................................................... 41
  4.2 Latched Comparator .................................................................................... 44
  4.3 Differential Binary-weighted Capacitor Array ........................................... 44
  4.3 Registers Utilized in Control Logic Module, State Machine and Shift Registers .. 48
  4.4 Control Logic Module ................................................................................ 49
  4.5 Other Considerations .................................................................................. 50

CHAPTER 5: SIMULATION RESULTS .................................................................... 51
  5.1 ADC Functionality Verification .................................................................... 51
  5.2 Power Consumption ..................................................................................... 52

CHAPTER 6: CONCLUSION ................................................................................. 55

BIBLIOGRAPHY ................................................................................................ 56

CURRICULUM VITAE .......................................................................................... 57
LIST OF TABLES

Table 2.1 Relationship between B7-X and the connection of capacitors C26-X_2/1±. (1 ≤ X ≤ 6). ................................................................................................................................................. 15

Table 2.2 Connection table for C32_2/1±................................................................................................. 17

Table 2.3 Connection table for C16_2/1±................................................................................................ 19

Table 2.4 Connection table for C8_2/1±.................................................................................................. 22

Table 2.5 Connection table for C4_2/1±.................................................................................................. 24

Table 2.6 Connection table for C2_2/1±.................................................................................................. 26

Table 2.7 Connection table for C1_4/3±.................................................................................................. 28

Table 4.1 Layout information .................................................................................................................. 41
LIST OF FIGURES

Fig. 1.1 Power versus sampling rate for different types of ADC, referenced from [3] ..... 2

Fig. 2.1 System block diagram. ......................................................................................... 4

Fig. 2.2 Schematic of latched comparator. ........................................................................... 5

Fig. 2.3 Schematic of differential binary-weighted capacitor array. .................................. 8

Fig. 2.4 The second MSB capacitor is split into a bunch of binary-weighted sub-capacitors... 9

Fig. 2.5 System timing diagram .......................................................................................... 10

Fig. 2.6 The connection (switched by control logic) of capacitor array during #Sample. 11

Fig. 2.7 Simulated waveforms of the ADC in this work (for Vin = 820mV). .................... 11

Fig. 2.8 The connection (switched by control logic) of capacitor array during #BC0. .... 12

Fig. 2.9 The connection (switched by control logic) of capacitor array during #BC1. .... 13

Fig. 2.10 The equivalent simplified circuit for Fig. 2.9....................................................... 15

Fig. 2.11 Simulated waveforms of the ADC in this work (for Vin = 820mV), zoom-in
view for #BC1 – #BC7. ........................................................................................................ 17

Fig. 2.12 The connection (switched by control logic) of capacitor array during #BC2. .. 17

Fig. 2.13 The equivalent simplified circuit for Fig. 2.12...................................................... 18

Fig. 2.14 The connection (switched by control logic) of capacitor array during #BC3. .. 20

Fig. 2.15 The equivalent simplified circuit for Fig. 2.14...................................................... 20

Fig. 2.16 The connection (switched by control logic) of capacitor array during #BC4. .. 22

Fig. 2.17 The equivalent simplified circuit for Fig. 2.16...................................................... 22

Fig. 2.18 The connection (switched by control logic) of capacitor array during #BC5. .. 24

Fig. 2.19 The equivalent simplified circuit for Fig. 2.18...................................................... 24
Fig. 2.20 The connection (switched by control logic) of capacitor array during #BC6... 26
Fig. 2.21 The equivalent simplified circuit for Fig. 2.20................................. 26
Fig. 2.22 The connection (switched by control logic) of capacitor array during #BC7... 28
Fig. 2.23 The equivalent simplified circuit for Fig. 2.22.................................... 28
Fig. 2.24 Transient response: the simulated waveforms of some nodes worthy of attention
   (for Vin = 820mV)......................................................................................... 30
Fig. 2.25 Control logic......................................................................................... 33
Fig. 2.26 A master-slave edge-triggered D flip-flop is used as the register.............. 34
Fig. 2.27 State machine..................................................................................... 34
Fig. 2.28 Shift registers..................................................................................... 35
Fig. 3.1 Conventional capacitor array............................................................... 36
Fig. 3.2 A 2-bit capacitor array........................................................................... 37
Fig. 3.3 A downward correction in conventional SAR algorithm.......................... 38
Fig. 3.4 A downward correction in energy-efficiency algorithm............................ 39
Fig. 4.1 Layout of ADC, with marked circuit blocks.......................................... 41
Fig. 4.2 Layout of ADC .................................................................................. 42
Fig. 4.3 Zoomed-in layout of latched comparator (CMP) and one of control logic
   modules in the whole ADC............................................................................. 43
Fig. 4.4 Layout of latched comparator (CMP)..................................................... 44
Fig. 4.5 Layout of positive capacitor array.......................................................... 45
Fig. 4.6 Layout illustration of the capacitor array (for both positive and negative arrays). 46
Fig. 4.7 Connection of the capacitor array with logic control modules using highlight wirings
Fig. 4.8 Layout of register
Fig. 4.9 Layout of the logic circuit controlling C128+ and C128-
Fig. 4.10 Layout of the logic circuit controlling C32 – C1
Fig. 5.1 The circuit used for simulation
Fig. 5.2 Simulation Result acquired from QRC model of layout
Fig. 5.3 The current waveform of the power supply VDD (for Vin = 62mV)
Fig. 5.4 The current waveform of the power supply VDD (for Vin = 820mV)
CHAPTER 1: BACKGROUND

1.1 Neural Recorder Chip

There is a tremendous interest today in studying the behavior and bio-electronic function of the human brain, and in developing a brain-machine interface, such that persons with injuries causing paralysis or diseases such as Parkinson’s and Alzheimer’s might be able to regain cognitive and bodily functions. One avenue of research employs designing chips with probes to actual neurons in the brain (or regions in the brain) so that neural signals such as active neuron spikes and/or local field potentials can be observed on a screen outside the brain and further studied.

Since battery power is generally not possible for powering chips of this nature, power is provided by RF far-field (or near-field) radiation using a wireless rectifier (or perhaps even by optical fiber link), requiring the neural sensor chip to operate on a very low power budget. Specifically, all the circuitry on a wireless neural sensor IC, including neural signal amplifier, A/D converter (ADC), modulator, and RF transmitter must live with a total DC power of less than 1-mW, and often as low as 100-µW.

Many neural sensor arrays sample the analog neural signal and then convert it to the digital domain based on a low-power ADC. The sampled digital neural signal is then transmitted to a nearby receiver and PC, using either backscattered RF energy or a very low power RF transmitter, with a matched antenna to represent a “1” and a shorted antenna to represent a “0”.

Therefore, ADC is the key component in a neural recorder chip, ensuring the value of the analog neural signal can be accurately processed by digital modules.
1.2 Requirements for ADC Design in Neural Recorder Chip

Accuracy, speed and power consumption are the three main aspects in terms of requirements for ADC design in neural recorder chip.

1. Accuracy: Generally, 8-bit conversion is enough for most applications.

2. Speed: Since the frequency spectrum of a neural spike (action potential) is generally 10Hz – 10kHz, according to sampling theorem, sampling can be done at a conversion rate of 20kHz – 50kHz.

3. Power consumption: As is mentioned above, the main task is to realize low power design, and thereby the ADC should operate with a power consumption less than 100-µW (less than 20-µW in this work), from a 1-V power source.

1.3 ADC Type Comparison

Fig. 1.1 (referenced from [3]) shows the condition of power versus sampling rate for different types of ADC.

![Fig. 1.1 Power versus sampling rate for different types of ADC, referenced from [3].](image-url)
Apparently, Flash ADC has the fastest speed while consumes the maximum power compared with other types. Folding, Half-Flash and Pipelined ADC sacrifices speed to some extent for lower power consumption, but still too much for neural recorder applications. Sigma-Delta ADC has an advantage of outstanding accuracy (e.g. accurate 12-bit conversion is possible for Sigma-Delta structure) but suffers low sampling frequency.

Discussion in Section 1.2 reveals that 8-bit conversion and not so fast speed is moderate for the ADC in neural recorder applications, where reducing power dissipation is the most significant consideration. As a matter of fact, Fig. 1.1 indicates that SAR ADC is a perfect compromise for accuracy, speed and power consumption. Therefore, SAR structure is chosen in this work to realize the ADC.
CHAPTER 2: CIRCUIT DESIGN

2.1 System Block Diagram

As is shown in Fig. 2.1, the proposed low-power SAR-ADC consists of (1) a latched comparator, (2) a modified differential binary-weighted capacitor array based on charge redistribution to realize energy-efficiency, (3) a state machine and related control logic module and (4) shift registers for digital output.

Fig. 2.1 System block diagram.

2.2 Latched Comparator

The output of a continuous comparator should always tracks the input signal, which indicates a continuous comparison. However, as far as ADC is concerned, comparator is required only at certain periods of time. Thus, a comparator with a clocked input (i.e. dynamic comparator) shall operate comparison under control.

On the other hand, considering low-power design, continuous comparators cannot get rid of static power (i.e. the DC biasing consumption of amplifier used as comparator)
while dynamic comparators only consume dynamic power when comparing and pre-charging (i.e. no DC consumption when disabled).

Therefore, a latched comparator that has a clocked input is utilized here and its circuit is shown in Fig. 2.2.

![Fig. 2.2 Schematic of latched comparator.](image)

The principle of this latched comparator (CMP) can be described as:

1. **Pre-charge Phase**: CMP\_clk = 0

   N0 is OFF; P1, P2 and P0 are all ON.

   Under this circumstance, node CMP\_Vout+ and CMP\_Vout- are pulled up by P2 and P1 to Vdd respectively, with P0 ensuring a short path for these 2 nodes to avoid any potential difference.

   Since N0 is OFF, there is no current path from Vdd to GND through P3, N3, N1, N0 and through P4, N4, N2, N0. Thus, no power consumption exists after node CMP\_Vout+ and CMP\_Vout- are already charged to Vdd.

   This procedure is regarded as the pre-charge phase.
2. **Comparison Phase**: CMP_clk = 1

   N0 is ON; P1, P2 and P0 are all OFF.

   Under this circumstance, node CMP_Vout+ and CMP_Vout- are disconnected to Vdd.

   As a matter of fact, P3 and N3 constitute a digital inverter, and so do P4 and N4. Consequently, a pair of back-to-back inverters that can perform a strong positive feedback results.

   That is to say, if there is an effective potential difference between node CMP_Vin+ and CMP_Vin-, N1 or N2 will have a larger $V_{GS}$ which breaks the balance between the left path (N1 side) and the right path (N2 side), i.e. the NMOS with a larger $V_{GS}$ will become more conductive and thus be pulled down to GND more quickly. Then, as soon as the small difference between node CMP_Vout+ and CMP_Vout- is enough to set the positive-feedback back-to-back inverters, i.e. to set the latch, one of node CMP_Vout+ and CMP_Vout- will be set to “1” (Vdd) while the other one is pulled down to “0” (GND). In other words, the comparison result is thereby revealed, i.e.

   If CMP_Vin+ > CMP_Vin-: CMP_Vout- = 0, CMP_Vout+ = 1

   If CMP_Vin+ < CMP_Vin-: CMP_Vout- = 1, CMP_Vout+ = 0

   Therefore, node CMP_Vout+ represents comparison result based on positive logic.

   Once the latch is set, since the NMOS and PMOS in an inverter cannot be both ON, there is no current path from Vdd to GND through P3, N3, N1, N0 and
through \(P4, N4, N2, N0\). Thus, power consumption only exists during transition. This procedure is regarded as the comparison phase.

### 2.3 Differential Binary-weighted Capacitor Array

Considering a traditional charge redistribution ADC, if the bit cycling result indicates an upward approximation-voltage correction (input-voltage > approximation-voltage), more charges will be put onto the capacitor array. However, if a downward approximation-voltage correction is needed (input-voltage < approximation-voltage), according to the conventional algorithm of ADC, it will merely throw away some charges that have been stored on the capacitors, to generate the desired smaller approximation-voltage.

Not surprisingly, the charge thrown away has been totally wasted. To have a better understanding of this, assume that there is a circuit structure to store the charges that may originally be thrown away, during the downward correction. Thus, if a downward correction happens in current bit cycling and there is an upward correction required in next bit cycling, instead of only from the power supply, the capacitor array will be charged from these stored charges as well. Therefore, the energy is saved.

As is mathematically obvious, the downward correction accounts for half of the situations in every bit cycling. In conclusion, the analysis above reveals a lack of energy efficiency in traditional structure of charge redistribution ADC since it has no mechanism to store the charges but simply throws them away in a downward correction.
Papers concerning energy-saving methodologies in capacitor array have been proposed these years \([1][2]\). Inspired by these papers, the design in this work realizes the mentioned charge reuse mechanism by splitting the second MSB capacitor of the capacitor array into a bunch of binary-weighted sub-capacitors in parallel. (More details on how it works will be given in the following discussions.)

On the other hand, in order to suppress the common-mode noise, the design implements a differential capacitor array, which matches the differential input structure of the latched comparator (CMP). Moreover, the influence of parasitic capacitance on input nodes of the comparator can be eliminated thanks to the differential structure.

Thus, a modified differential binary-weighted capacitor array that can accomplish energy-efficiency results, as is shown in Fig. 2.3.

![Fig. 2.3 Schematic of differential binary-weighted capacitor array.](image)

Since the accuracy of charge redistribution ADC is determined by the matching quality of the capacitor array, the larger binary-weighted capacitor is constituted by a number of unit capacitors. The value of the unit capacitor should be satisfied with (1) short charging time (i.e. enough conversion rate), (2) small area needed for layout and fabrication, (3) small voltage change caused by charge loss on capacitors during conversion and (4) insensitivity to parasitic effects. Note that (1) and (2) call for small capacitance while (3) and (4) are for the purpose of good accuracy and linearity so they
call for big capacitance. Given all these factors and meanwhile considering the process of 8HP technology used in this design, a unit metal-insulator-metal (MIM) capacitor of 40fF (6.2µm × 6.2µm) is chosen here.

An 8-bit conversion requires a MSB capacitor that has the maximum capacitance equal to \(2^{8-1} = 128\) times the value of the unit capacitance (40fF), i.e. \(40\text{fF} \times 128 = 5.12\text{pF}\). Consequently, the second MSB capacitor should be 2.56pF. As is mentioned above, the second MSB capacitor should be split into a bunch of binary-weighted sub-capacitors, which is clearly marked by the black frames in Fig. 2.4.

![Fig. 2.4 The second MSB capacitor is split into a bunch of binary-weighted sub-capacitors.](image)

To explain this modified structure compared with traditional capacitor array, consider the equation

\[ 64 = 32 + 16 + 8 + 4 + 2 + 1 + 1 \]

Traditional capacitor array should consist of C128, C64, C32, C16, C8, C4, C2, C1 and C1. Now, the second MSB capacitor C64 is split into these capacitors with black frames: C32, C16, C8, C4, C2, C1 and C1, which are just identical to the capacitors without black frames next to them (except the MSB capacitor C128).
System timing diagram is shown here in Fig. 2.5. For one sampled voltage, completely 9 clock cycles (i.e. $1 \times \text{Sample} + 8 \times \text{Bit Cycling}$) are needed to finish the 8-bit A/D conversion.

![System Timing Diagram](image)

In order to more comprehensibly show how the modified capacitor array works, assume that we have an analog voltage of 820mV as the input signal. The following discussion will cover the control logic (which is much different from the conventional control logic) associated with the capacitor array during the 9 clock cycles. Furthermore, significant node voltages during each clock cycle will be calculated according to circuit principle. Then, a simulated result from actual implemented circuit (this work) will be given, which will finally be compared to those calculated theoretical values. Thus, the validity of the split structure of the second MSB capacitor, i.e. the modified energy-saving capacitor array, can be proved.

$V_{\text{ref}}$ in this work represents $\frac{1}{2} V_{\text{dd}}$. Since $V_{\text{dd}} = 1V$, $V_{\text{ref}} = 0.5V$.

Analog Input: $V_{in} = 820$ mV.

1. **Sample**, i.e. the 1st clock cycle

   Switched by control logic (which is omitted here for simplification and will be
further discussed later in a specific section), the connection of capacitor array during Sample is shown below in Fig. 2.6.

![Fig. 2.6 The connection (switched by control logic) of capacitor array during #Sample.](image)

CMP_Vin+ (i.e. the top plates of positive capacitor array) is connected to Vdd while the bottom plates of positive capacitor array are all connected to Vin. Thus, the charge \( Q_+ = C_{256} (Vdd - Vin) = C_{256} (1 - 0.82) = (1 - 0.82)C_{256} \) is stored in positive capacitor array.

CMP_Vin- (i.e. the top plates of negative capacitor array) is connected to Vref while the bottom plates of negative capacitor array are all connected to GND. Thus, the charge \( Q_- = C_{256} (Vref - GND) = C_{256} (0.5 - 0) = (1 - 0.5)C_{256} \) is stored in negative capacitor array.

![Fig. 2.7 Simulated waveforms of the ADC in this work (for Vin = 820mV).](image)
During *Sample*, based on the above theoretical reasoning, CMP\_Vin+ = 1V while CMP\_Vin- = 0.5V. Fig. 2.7 in the previous page shows the simulated waveforms of the actual circuit, in which M0 (1.0V) and M1 (496.1mV) correspond with the theoretical values very well.

2. *Bit Cycling 0 (BC0)*, i.e. the 2nd clock cycle

The connection of capacitor array during BC0 is shown in Fig. 2.8.

![Fig. 2.8 The connection (switched by control logic) of capacitor array during #BC0.](image)

CMP\_Vin+ (i.e. the top plates of positive capacitor array) is disconnected to Vdd (this disconnection remains in subsequent 7 Bit Cyclings, which will not be mentioned again for conciseness) while the bottom plates of positive capacitor array are all connected to GND. As node CMP\_Vin+ is open now, no charge can be moved to anywhere and thereby the bottom plates of positive capacitor array (GND) may force node CMP\_Vin+ to be \( \frac{(1 - 0.82)C_{256}}{C_{256}} = (1 - 0.82)V = 0.18V \).

Also, CMP\_Vin- (i.e. the top plates of negative capacitor array) is disconnected to Vref (this disconnection remains in subsequent 7 Bit Cyclings, which will not be mentioned again for conciseness) while the bottom plates of negative capacitor array are all connected to GND. As node CMP\_Vin- is open now, no charge can be moved to anywhere and thereby the bottom plates of negative capacitor array
(GND) may force node CMP Vin- to be \( \frac{(1 - 0.5)C_{256}}{C_{256}} = (1 - 0.5)V = 0.5V. \)

Thus, it indicates that during BC0, 0.18V is compared with 0.5V. In other words, 0.82V is compared with 0.5V.

Consequently, the comparator (CMP) will reveal the result that

\[ 0.82V > 0.5V \]

Therefore, MSB (the 7th bit \( B_7 \)) of the final digital output will be a “1”, and for the time being,

\[ \text{Digital Output} = B_7B_6B_5B_4B_3B_2B_1B_0 = 1XXX XXXX \]

During BC0, based on the above theoretical reasoning, CMP Vin+ = 0.18V while CMP Vin- = 0.5V. Fig. 2.7 shows the simulated waveforms of the actual circuit, in which M3 (181.3mV) and M2 (499.4mV) correspond with the theoretical values very well.

3. **Bit Cycling 1 (BC1)**, i.e. the 3rd clock cycle

The connection of capacitor array during BC1 is shown in Fig. 2.9.

![Fig. 2.9](image)

Note that (for both positive and negative array) the bottom plates of the capacitors split from C64 (i.e. the capacitors with black frames in Fig. 2.4) are connected to Vref, while the capacitors of identical values next to them are
connected to GND.

Interestingly, from another perspective, if one capacitor of positive array is connected to Vref (e.g. C32_2+), the capacitor located under it of negative array must be connected to GND (e.g. C32_2-), and vice versa (e.g. C32_1+ and C32_1-). This special structure, or so-called *Complementary Pattern*, exists for all the situations during BC1 – BC7.

If there are no C128+ and C128-, since the equivalent total capacitor connected to Vref is equal to the equivalent total capacitor connected to GND (for both positive and negative array), node CMP_Vin+ and CMP_Vin- will be $\frac{1}{2}$ Vref, which indicates a balanced input (i.e. differential input = 0) for the comparator (CMP).

Nevertheless, as a matter of fact, C128+ is connected to Vref while C128- is connected to GND. This connection is determined by the result from the previous Bit Cycling (BC0), i.e. the result of “1” for MSB sets C128+ to be Vref and sets C128- to be GND. (On the other hand, if the result for MSB is a “0”, C128+ will be set to be GND and C128- will be set to be Vref. Thus, C128+ and C128- also follow *Complementary Pattern*.)

Similarly, it is necessary to present a more general feature here: The converted bit $B_{7,X}$ acquired from Bit Cycling X (BCX) will determine the connection of the subsequent binary-weighted capacitors $C_{2^6,X \_2/1\pm}$, i.e.
Table 2.1 Relationship between $B_{7-X}$ and the connection of capacitors $C^{6-X}_{2/1\pm}$.

<table>
<thead>
<tr>
<th>The connection of $C^{6-X}_{2/1\pm}$</th>
<th>IF $B_{7-X} = 1$</th>
<th>IF $B_{7-X} = 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C^{6-X}_{2+}$</td>
<td>Vref (No change)</td>
<td>GND</td>
</tr>
<tr>
<td>$C^{6-X}_{2-}$</td>
<td>GND (No change)</td>
<td>Vref</td>
</tr>
<tr>
<td>$C^{6-X}_{1+}$</td>
<td>Vref</td>
<td>GND (No change)</td>
</tr>
<tr>
<td>$C^{6-X}_{1-}$</td>
<td>GND</td>
<td>Vref (No change)</td>
</tr>
</tbody>
</table>

When all the 8 bits are completely digitalized after $BC7$, no more connection alteration is needed, and thereby $1 \leq X \leq 6$. (Note that $B_7$ acquired from $BC0$ ($X = 0$) which determines $C128+$ and $C128-$ is already discussed above.)

Precisely speaking, there is a small difference for $X = 6$, i.e. when it comes to $X = 6$, $C1_{2+}$, $C1_{2-}$, $C1_{1+}$ and $C1_{1-}$ in Table 2.1 should be replaced by $C1_{4+}$, $C1_{4-}$, $C1_{3+}$ and $C1_{3-}$, respectively.

Last but not least, as can be observed in Table 2.1, Complementary Pattern for positive and negative array is still satisfied. This is a meaningful property to take into consideration when implementing circuits for control logic.

To calculate the voltage of node CMP_Vin+ and CMP_Vin- during $BC1$, the equivalent simplified circuit for Fig. 2.9 is shown in Fig. 2.10.

Fig. 2.10 The equivalent simplified circuit for Fig. 2.9.
As node CMP_Vin+ is always open now, the charge accumulated on the top plates of positive capacitor array during Sample cannot be moved to anywhere. Accordingly, CMP_Vin+ should be
\[
\frac{(1 - 0.82)C_{256}}{C_{256}} + \frac{128 + 64}{(128 + 64) + 64} V_{\text{ref}} = [1 - (0.82 - \frac{3}{8})]V = 0.555V
\]

Also, as node CMP_Vin- is always open now, the charge accumulated on the top plates of negative capacitor array during Sample cannot be moved to anywhere. Accordingly, CMP_Vin- should be
\[
\frac{(1 - 0.5)C_{256}}{C_{256}} + \frac{64}{(128 + 64) + 64} V_{\text{ref}} = [1 - (0.5 - \frac{1}{8})]V = 0.625V
\]

Thus, it indicates that during BC1, 0.555V is compared with 0.625V. In other words,
\[
(0.82 - \frac{3}{8})V \text{ is compared with } (0.5 - \frac{1}{8})V
\]

i.e. 0.82V is compared with \((\frac{1}{2} + \frac{1}{4})V\)

Consequently, the comparator (CMP) will reveal the result that
\[
0.82V > (\frac{1}{2} + \frac{1}{4})V
\]

Therefore, the 6th bit \(B_6\) of the final digital output will be a “1”, and for the time being,

Digital Output = \(B_7B_6B_5B_4B_3B_2B_1B_0\) = 11XX XXXX

During BC1, based on the above theoretical reasoning, CMP_Vin+ = 0.555V while CMP_Vin- = 0.625V. Fig. 2.11 in the next page shows the simulated waveforms of the actual circuit, in which M1 (556mV) and M0 (624.2mV)
correspond with the theoretical values very well.

Fig. 2.11 Simulated waveforms of the ADC in this work (for Vin = 820mV), zoom-in view for #BC1 – #BC7.

4. *Bit Cycling 2 (BC2)*, i.e. the 4th clock cycle

Based on Table 2.1, since $B_6 = 1$,

<table>
<thead>
<tr>
<th>The connection of</th>
<th>$B_6 = 1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>C32_2+</td>
<td>Vref (No change)</td>
</tr>
<tr>
<td>C32_2-</td>
<td>GND (No change)</td>
</tr>
<tr>
<td>C32_1+</td>
<td>Vref</td>
</tr>
<tr>
<td>C32_1-</td>
<td>GND</td>
</tr>
</tbody>
</table>

Table 2.2 Connection table for C32_2/1±.

Thus, the connection of capacitor array during BC2 is shown in Fig. 2.12. The only alteration compared with the connection during BC1 (Fig. 2.9) is marked by a black frame, i.e. C32_1+ is connected to Vref and C32_1- is connected to GND.

Fig. 2.12 The connection (switched by control logic) of capacitor array during #BC2.
To calculate the voltage of node CMP_Vin+ and CMP_Vin- during BC2, the equivalent simplified circuit for Fig. 2.12 is shown in Fig. 2.13.

![Fig. 2.13 The equivalent simplified circuit for Fig. 2.12.](image)

As node CMP_Vin+ is always open now, the charge accumulated on the top plates of positive capacitor array during Sample cannot be moved to anywhere. Accordingly, CMP_Vin+ should be

\[
\frac{(1 - 0.82)C_{256}}{C_{256}} + \frac{128 + 64 + 32}{256} \text{V}_{\text{ref}} = [1 - (0.82 - \frac{7}{16})]V = 0.6175V
\]

Also, as node CMP_Vin- is always open now, the charge accumulated on the top plates of negative capacitor array during Sample cannot be moved to anywhere. Accordingly, CMP_Vin- should be

\[
\frac{(1 - 0.5)C_{256}}{C_{256}} + \frac{32}{256} \text{V}_{\text{ref}} = [1 - (0.5 - \frac{1}{16})]V = 0.5625V
\]

Thus, it indicates that during BC2, 0.6175V is compared with 0.5625V. In other words,

\[(0.82 - \frac{7}{16})V \text{ is compared with } (0.5 - \frac{1}{16})V\]

i.e. 0.82V is compared with \(\frac{1}{2} + \frac{1}{4} + \frac{1}{8}\)V

Consequently, the comparator (CMP) will reveal the result that
\[ 0.82V < \left( \frac{1}{2} + \frac{1}{4} + \frac{1}{8} \right)V \]

Therefore, the 5th bit \( B_5 \) of the final digital output will be a “0”, and for the time being,

\[
\text{Digital Output} = B_7B_6B_5B_4B_3B_2B_1B_0 = 110X XXXX
\]

During \( BC2 \), based on the above theoretical reasoning, \( \text{CMP Vin}^+ = 0.6175V \) while \( \text{CMP Vin}^- = 0.5625V \). Fig. 2.11 shows the simulated waveforms of the actual circuit, in which \( M2 (618.5mV) \) and \( M3 (561.8mV) \) correspond with the theoretical values very well.

5. **Bit Cycling 3 (BC3)**, i.e. the 5th clock cycle

Based on Table. 2.1, since \( B_5 = 0 \),

<table>
<thead>
<tr>
<th>The connection of</th>
<th>( B_5 = 0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>C16_2+</td>
<td>GND</td>
</tr>
<tr>
<td>C16_2-</td>
<td>Vref</td>
</tr>
<tr>
<td>C16_1+</td>
<td>GND (No change)</td>
</tr>
<tr>
<td>C16_1-</td>
<td>Vref (No change)</td>
</tr>
</tbody>
</table>

Table. 2.3 Connection table for C16_2/1±.

Thus, the connection of capacitor array during \( BC3 \) is shown in Fig. 2.14 in the next page. The only alteration compared with the connection during \( BC2 \) (Fig. 2.12) is marked by a black frame, i.e. \( \text{C16}_2^+ \) is connected to GND and \( \text{C16}_2^- \) is connected to Vref.

As far as the traditional structure for capacitor array is concerned, if the result acquired from the previous Bit Cycling is a “0” and thereby indicates a downward
approximation-voltage correction, there must be proper operations to reset the previous binary-weighted capacitors, i.e. to reconnect them to their original positions.

Fig. 2.14 The connection (switched by control logic) of capacitor array during #BC3.

However, according to Table. 2.1 (which reveals the alteration of capacitor connection), no such reset operation is needed for the proposed modified structure, owing to the cooperation of those binary-weighted sub-capacitors split from C64 (i.e. by setting the connection of the next binary-weighted capacitors, downward approximation-voltage correction can also be realized), which is definitely another advantage for designing circuit of control logic.

To calculate the voltage of node CMP_Vin+ and CMP_Vin- during BC3, the equivalent simplified circuit for Fig. 2.14 is shown in Fig. 2.15.

Fig. 2.15 The equivalent simplified circuit for Fig. 2.14.

As node CMP_Vin+ is always open now, the charge accumulated on the top
plates of positive capacitor array during Sample cannot be moved to anywhere.

Accordingly, CMP_Vin+ should be

\[
\frac{(1 - 0.82)C_{256}}{C_{256}} + \frac{128 + 48 + 32}{256} V_{ref} = [1 - (0.82 - \frac{13}{32})]V = 0.5862V
\]

Also, as node CMP_Vin- is always open now, the charge accumulated on the top plates of negative capacitor array during Sample cannot be moved to anywhere.

Accordingly, CMP_Vin- should be

\[
\frac{(1 - 0.5)C_{256}}{C_{256}} + \frac{32 + 16}{256} V_{ref} = [1 - (0.5 - \frac{3}{32})]V = 0.5938V
\]

Thus, it indicates that during BC3, 0.5862V is compared with 0.5938V. In other words,

\[
(0.82 - \frac{13}{32})V \text{ is compared with } (0.5 - \frac{3}{32})V
\]

i.e. 0.82V is compared with \((\frac{1}{2} + \frac{1}{4} + \frac{1}{16})V\)

Consequently, the comparator (CMP) will reveal the result that

\[
0.82V > (\frac{1}{2} + \frac{1}{4} + \frac{1}{16})V
\]

Therefore, the 4th bit \(B_4\) of the final digital output will be a “1”, and for the time being,

\[
\text{Digital Output} = B_7B_6B_5B_4B_3B_2B_1B_0 = 1101 \text{ XXXX}
\]

During BC3, based on the above theoretical reasoning, CMP_Vin+ = 0.5862V while CMP_Vin- = 0.5938V. Fig. 2.11 shows the simulated waveforms of the actual circuit, in which M5 (587.3mV) and M4 (593.1mV) correspond with the theoretical values very well.
6. *Bit Cycling 4 (BC4)*, i.e. the 6th clock cycle

Based on Table. 2.1, since \( B_4 = 1 \),

<table>
<thead>
<tr>
<th>The connection of</th>
<th>( B_4 = 1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>C8_2+</td>
<td>Vref (No change)</td>
</tr>
<tr>
<td>C8_2-</td>
<td>GND (No change)</td>
</tr>
<tr>
<td>C8_1+</td>
<td>Vref</td>
</tr>
<tr>
<td>C8_1-</td>
<td>GND</td>
</tr>
</tbody>
</table>

Table. 2.4 Connection table for C8_2/1±.

Thus, the connection of capacitor array during *BC4* is shown in Fig. 2.16. The only alteration compared with the connection during *BC3* (Fig. 2.14) is marked by a black frame, i.e. C8_1+ is connected to Vref and C8_1- is connected to GND.

![Fig. 2.16 The connection (switched by control logic) of capacitor array during #BC4.](image)

To calculate the voltage of node CMP_Vin+ and CMP_Vin- during *BC4*, the equivalent simplified circuit for Fig. 2.16 is shown in Fig. 2.17.

![Fig. 2.17 The equivalent simplified circuit for Fig. 2.16.](image)
As node CMP_Vin+ is always open now, the charge accumulated on the top plates of positive capacitor array during Sample cannot be moved to anywhere.

Accordingly, CMP_Vin+ should be

\[
\frac{(1 - 0.82)C_{256}}{C_{256}} + \frac{128 + 48 + 32 + 8}{256}V_{\text{ref}} = [1 - (0.82 - \frac{27}{64})]V = 0.6019V
\]

Also, as node CMP_Vin- is always open now, the charge accumulated on the top plates of negative capacitor array during Sample cannot be moved to anywhere.

Accordingly, CMP_Vin- should be

\[
\frac{(1 - 0.5)C_{256}}{C_{256}} + \frac{24 + 16}{256}V_{\text{ref}} = [1 - (0.5 - \frac{5}{64})]V = 0.5781V
\]

Thus, it indicates that during BC4, 0.6019V is compared with 0.5781V. In other words,

\[
(0.82 - \frac{27}{64})V \text{ is compared with } (0.5 - \frac{5}{64})V
\]

i.e. 0.82V is compared with \(\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{32}\)V

Consequently, the comparator (CMP) will reveal the result that

\[0.82V < \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{32}\right)V\]

Therefore, the 3rd bit \(B_3\) of the final digital output will be a “0”, and for the time being,

Digital Output = \(B_7B_6B_5B_4B_3B_2B_1B_0 = 1101\) 0XXX

During BC4, based on the above theoretical reasoning, CMP_Vin+ = 0.6019V while CMP_Vin- = 0.5781V. Fig. 2.11 shows the simulated waveforms of the actual circuit, in which M6 (603mV) and M7 (577.4mV) correspond with the
theoretical values very well.

7. *Bit Cycling 5 (BC5)*, i.e. the 7th clock cycle

Based on Table. 2.1, since $B_3 = 0$,

<table>
<thead>
<tr>
<th>The connection of</th>
<th>$B_3 = 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>C4_2+</td>
<td>GND</td>
</tr>
<tr>
<td>C4_2-</td>
<td>Vref</td>
</tr>
<tr>
<td>C4_1+</td>
<td>GND (No change)</td>
</tr>
<tr>
<td>C4_1-</td>
<td>Vref (No change)</td>
</tr>
</tbody>
</table>

Table. 2.5 Connection table for C4_2/1±.

Thus, the connection of capacitor array during BC5 is shown in Fig. 2.18. The only alteration compared with the connection during BC4 (Fig. 2.16) is marked by a black frame, i.e. C4_2+ is connected to GND and C4_2- is connected to Vref.

![Fig. 2.18 The connection (switched by control logic) of capacitor array during #BC5.](image)

To calculate the voltage of node CMP_Vin+ and CMP_Vin- during BC5, the equivalent simplified circuit for Fig. 2.18 is shown in Fig. 2.19.

![Fig. 2.19 The equivalent simplified circuit for Fig. 2.18.](image)
As node CMP_Vin+ is always open now, the charge accumulated on the top plates of positive capacitor array during Sample cannot be moved to anywhere. Accordingly, CMP_Vin+ should be

\[
\frac{(1 - 0.82)C_{256}}{C_{256}} + \frac{128 + 44 + 32 + 8}{256} V_{ref} = \left[1 - (0.82 - \frac{53}{128})\right]V = 0.5941V
\]

Also, as node CMP_Vin- is always open now, the charge accumulated on the top plates of negative capacitor array during Sample cannot be moved to anywhere. Accordingly, CMP_Vin- should be

\[
\frac{(1 - 0.5)C_{256}}{C_{256}} + \frac{24 + 16 + 4}{256} V_{ref} = \left[1 - (0.5 - \frac{11}{128})\right]V = 0.5859V
\]

Thus, it indicates that during BC5, 0.5941V is compared with 0.5859V. In other words,

\[
(0.82 - \frac{53}{128})V \text{ is compared with } (0.5 - \frac{11}{128})V
\]

i.e. 0.82V is compared with \((\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{64})V\)

Consequently, the comparator (CMP) will reveal the result that

\[
0.82V < (\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{64})V
\]

Therefore, the 2nd bit \(B_2\) of the final digital output will be a “0”, and for the time being,

Digital Output = \(B_7B_6B_5B_4B_3B_2B_1B_0 = 1101\) 00XX

During BC5, based on the above theoretical reasoning, CMP_Vin+ = 0.5941V while CMP_Vin- = 0.5859V. Fig. 2.11 shows the simulated waveforms of the actual circuit, in which M8 (595.2mV) and M9 (585.1mV) correspond with the
theoretical values very well.

8. **Bit Cycling 6 (BC6)**, i.e. the 8th clock cycle

Based on Table. 2.1, since \( B_2 = 0 \),

<table>
<thead>
<tr>
<th>The connection of</th>
<th>( B_2 = 0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{2,2}^+ )</td>
<td>GND</td>
</tr>
<tr>
<td>( C_{2,2}^- )</td>
<td>Vref</td>
</tr>
<tr>
<td>( C_{2,1}^+ )</td>
<td>GND (No change)</td>
</tr>
<tr>
<td>( C_{2,1}^- )</td>
<td>Vref (No change)</td>
</tr>
</tbody>
</table>

Table. 2.6 Connection table for \( C_{2,2}/1^\pm \).

Thus, the connection of capacitor array during BC6 is shown in Fig. 2.20. The only alteration compared with the connection during BC5 (Fig. 2.18) is marked by a black frame, i.e. \( C_{2,2}^+ \) is connected to GND and \( C_{2,2}^- \) is connected to Vref.

Fig. 2.20 The connection (switched by control logic) of capacitor array during #BC6.

To calculate the voltage of node CMP\(_{\text{Vin}^+}\) and CMP\(_{\text{Vin}^-}\) during BC6, the equivalent simplified circuit for Fig. 2.20 is shown in Fig. 2.21.

Fig. 2.21 The equivalent simplified circuit for Fig. 2.20.
As node CMP_Vin+ is always open now, the charge accumulated on the top plates of positive capacitor array during Sample cannot be moved to anywhere. Accordingly, CMP_Vin+ should be

\[
\frac{(1 - 0.82)C_{256}}{C_{256}} + \frac{128 + 42 + 32 + 8}{256} \cdot V_{\text{ref}} = [1 - (0.82 - \frac{105}{256})]V = 0.5902V
\]

Also, as node CMP_Vin- is always open now, the charge accumulated on the top plates of negative capacitor array during Sample cannot be moved to anywhere. Accordingly, CMP_Vin- should be

\[
\frac{(1 - 0.5)C_{256}}{C_{256}} + \frac{24 + 16 + 4 + 2}{256} \cdot V_{\text{ref}} = [1 - (0.5 - \frac{23}{256})]V = 0.5898V
\]

Thus, it indicates that during BC6, 0.5902V is compared with 0.5898V. In other words,

\[(0.82 - \frac{105}{256})V \text{ is compared with } (0.5 - \frac{23}{256})V\]

i.e. 0.82V is compared with \((\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{128})V\)

Consequently, the comparator (CMP) will reveal the result that

\[0.82V < (\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{128})V\]

Therefore, the 1st bit \(B_1\) of the final digital output will be a “0”, and for the time being,

\[\text{Digital Output} = B_7B_6B_5B_4B_3B_2B_1B_0 = 1101 000X\]

During BC6, based on the above theoretical reasoning, CMP_Vin+ = 0.5902V while CMP_Vin- = 0.5898V. Fig. 2.11 shows the simulated waveforms of the actual circuit, in which M10 (591.4mV) and M11 (589mV) correspond with the
theoretical values very well.

9. **Bit Cycling 7 (BC7)**, i.e. the 9th clock cycle

Based on Table. 2.1, since $B_1 = 0$,

<table>
<thead>
<tr>
<th>The connection of</th>
<th>$B_1 = 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{1.4+}$</td>
<td>GND</td>
</tr>
<tr>
<td>$C_{1.4-}$</td>
<td>Vref</td>
</tr>
<tr>
<td>$C_{1.3+}$</td>
<td>GND (No change)</td>
</tr>
<tr>
<td>$C_{1.3-}$</td>
<td>Vref (No change)</td>
</tr>
</tbody>
</table>

Table. 2.7 Connection table for $C_{1.4/3\pm}$.

Thus, the connection of capacitor array during BC7 is shown in Fig. 2.22. The only alteration compared with the connection during BC6 (Fig. 2.20) is marked by a black frame, i.e. $C_{1.4+}$ is connected to GND and $C_{1.4-}$ is connected to Vref.

![Fig. 2.22 The connection (switched by control logic) of capacitor array during #BC7.](image)

To calculate the voltage of node CMP_Vin+ and CMP_Vin- during BC7, the equivalent simplified circuit for Fig. 2.22 is shown in Fig. 2.23.

![Fig. 2.23 The equivalent simplified circuit for Fig. 2.22.](image)
As node CMP_Vin+ is always open now, the charge accumulated on the top plates of positive capacitor array during Sample cannot be moved to anywhere. Accordingly, CMP_Vin+ should be

\[
\frac{(1 - 0.82)C_{256}}{C_{256}} + \frac{128 + 41 + 32 + 8}{256} V_{\text{ref}} = [1 - (0.82 - \frac{209}{512})]V = 0.5882V
\]

Also, as node CMP_Vin- is always open now, the charge accumulated on the top plates of negative capacitor array during Sample cannot be moved to anywhere. Accordingly, CMP_Vin- should be

\[
\frac{(1 - 0.5)C_{256}}{C_{256}} + \frac{24 + 16 + 4 + 2 + 1}{256} V_{\text{ref}} = [1 - (0.5 - \frac{47}{512})]V = 0.5918V
\]

Thus, it indicates that during BC7, 0.5882V is compared with 0.5918V. In other words,

\[(0.82 - \frac{209}{512})V \text{ is compared with } (0.5 - \frac{47}{512})V\]

i.e. 0.82V is compared with \(\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{256}\right)V\)

Consequently, the comparator (CMP) will reveal the result that

\[0.82V > \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{256}\right)V\]

Therefore, the 0th bit \(B_0\) of the digital output will be a “1”, and finally,

\[\text{Digital Output} = B_7B_6B_5B_4B_3B_2B_1B_0 = 1101\ 0001\]

During BC7, based on the above theoretical reasoning, CMP_Vin+ = 0.5882V while CMP_Vin- = 0.5918V. Fig. 2.11 shows the simulated waveforms of the actual circuit, in which M13 (589.5mV) and M12 (591.1mV) correspond with the theoretical values very well.
Acquired from the implemented circuit for $V_{in} = 820\text{mV}$, Fig. 2.24 below offers the simulated waveforms of some nodes worthy of attention.

As is shown in Fig. 2.24, clk and CMP_clk are input clock signals having a phase difference of $270^\circ$, based on system timing diagram.

Although the voltage of node CMP_Vin+ and CMP_Vin- are already given in Fig. 2.7 and Fig. 2.11 with clear values, they are provided here as a reference. In addition, the related clock cycles, i.e. Sample (abbreviated to SA) and $BC1 – BC7$, are listed to identify specific durations.
The discussion in Section 2.2 has pointed out that CMP_Vout+ represents comparison result based on positive logic. In other words, CMP_Vout- should represent comparison result based on negative logic. Meanwhile, the calculation made for the voltage of node CMP_Vin+ and CMP_Vin- reveals that we use a negative representation for the actual input voltage, so the comparison result is contrary to the actual situation. For instance, during BC7, according to the principle, we should compare 0.82V with 
\[ \left( \frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{256} \right)V, \] \[ \text{while in fact, we compared } [1 - (0.82 - \frac{209}{512})]V = 0.5882V \text{ with } [1 - (0.5 - \frac{47}{512})]V = 0.5918V, \] which can be further transformed to indicate that 
\[ -0.82V \text{ is compared with } -(\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{256})V. \]

Obviously, the comparison result for -0.82V with \(-\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{256}\right)V\) is contrary to the comparison result for 0.82V with \(\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{256}\right)V\). Thus, comparison result of the actual situation should be revealed by CMP_Vout-, since it is CMP_Vout- that represents comparison result based on negative logic.

CMP_Vout- is given in Fig. 2.24, but since it is a waveform of the analog node (i.e. the output node of the latched comparator), it cannot be treated as a pure digital waveform that has sharp rising and falling edges. Therefore, one additional register is connected to CMP_Vout-, to ensure that shifter registers for outputting digital bits, which are complete digital circuits, can get a clean digital input signal.

net0123 is the node Q of the first register in shift registers, which represents the bit acquired from previous Bit Cycling. Considering that all shift registers are triggered by the rising edge of clk and the conversion state (i.e. Sample and BC1 – BC7) is also
changed at the rising edge of clk, the bit acquired from previous Bit Cycling should appear on net0123 at the same time when the conversion state changes, which can be clearly observed in Fig. 2.24.

As a result, the final digital output according to the logic level of net0123 is:

\[ 1101 \ 0001 \]

which is exactly the same as the result inferred by the voltage of node CMP_Vin+ and CMP_Vin-.

In conclusion, by converting the final digital output back to its corresponding analog voltage

\[ (1101 \ 0001)_2 = \frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{256} = 816.4\text{mV} \]

and comparing this with

\[ (1101 \ 0010)_2 = \frac{1}{2} + \frac{1}{4} + \frac{1}{16} + \frac{1}{128} = 820.3\text{mV} > 820\text{mV} \]

the validity of the proposed ADC with modified capacitor array is proved, and thereby the voltage of quantization error \( V_x \) is

\[ V_x = 820 - 816.4 = 3.6\text{mV} < \frac{1}{256} \text{mV} (V_{\text{LSB}}) \]

Therefore, \( V_x \) is within a \( V_{\text{LSB}} \) as we expected, which is good enough, since there is a \( \frac{1}{2} \) LSB offset in practical ADC transfer characteristic compared with that of ideal ADC.

**2.4 Control Logic**

Control logic is the switches connecting capacitor array with Vs (from Vref/2 or Vin) or GND, which is shown in Fig 2.25 in the next page.
2.5 Other Digital Modules

Other digital modules include state machine and shift registers, which are shown in the following pages, with their core element – register (a master-slave edge-triggered D flip-flop).
Fig. 2.26 A master-slave edge-triggered D flip-flop is used as the register.

Fig. 2.27 State machine.
Fig. 2.28 Shift registers.
CHAPTER 3: ENERGY-EFFICIENCY ALGORITHM

3.1 Conventional SAR Algorithm

Section 2.3 has explained circuit operation of the modified capacitor array, i.e. how it works. To show the principle of energy-efficiency on which the modified capacitor array is based, i.e. why it works, first recall the conventional SAR algorithm. Fig. 3.1 below is the capacitor array in a conventional single-ended SAR-ADC, where $V_x$ is the input node of the comparator, $V_{\text{ref}}$ is connected to reference voltage and $V_{\text{in}}$ is the input analog voltage to be converted.

When conversion begins, firstly $S_{\text{Sample}} = 1$, so the voltage between two plates for all the capacitors should be $V_{\text{in}} - 0 = V_{\text{in}}$. Then, $S_{\text{Sample}}$ is open, thus the charge corresponding with $-V_{\text{in}}$ (choosing the top plate as the reference positive side) is stored on the capacitor array. Next, during 1st bit cycling, $C_b$ is connected to $V_{\text{ref}}$ while the other capacitors are all connected to GND. Consequently,
\[ V_x(1) = -V_{in} + \frac{V_{ref}}{2} \]

\( V_x \) is compared with 0 to determine whether an upward or downward correction is needed. If \( V_x < 0 \), \( V_x \) will be raised by connecting the 2\textsuperscript{nd} MSB capacitor \( C_{b-1} \) to \( V_{ref} \), i.e. an upward correction. Otherwise, \( C_b \) will be reconnected to GND while \( C_{b-1} \) will still be connected to \( V_{ref} \), i.e. a downward correction.

The process of bit cycling will be repeated \( b \) times until the last bit is achieved. After switching for each bit cycling,

\[ V_x = -V_{in} + \frac{C_{ref}}{C_{ref} + C_{GND}} V_{ref} \]

where \( C_{ref} \) is the total capacitance connected to \( V_{ref} \) and \( C_{GND} \) is the total capacitance connected to GND.

To alleviate the complexity of calculation for power consumption, assume we have a 2-bit capacitor array, which is shown in Fig. 3.2.

![Fig. 3.2 A 2-bit capacitor array.](image)
During 1st bit cycling, after S+(2) is connected to $V_{ref}$ and the capacitor array is completely settled when $V_x(1) = -V_{in} + \frac{V_{ref}}{2}$, the power drawn from $V_{ref}$ should be

$$E(\text{Sample} \rightarrow 1) = \int_0^t V_{ref} i_{ref}(t)dt = V_{ref} \int_0^t i_{ref}(t)dt = -V_{ref} \Delta Q$$

$$= -V_{ref} 2C_0[(V_x(1) - V_{ref}) - V_x(\text{Sample})] = C_0 V_{ref}^2$$

If $V_x < 0$, an upward correction will be operated and thereby,

$$V_x(2) = -V_{in} + \frac{3V_{ref}}{4}$$

$$E(1 \rightarrow 2) = -V_{ref} [2C_0[(V_x(2) - V_{ref}) - (V_x(1) - V_{ref})] + C_0[(V_x(2) - V_{ref}) - V_x(1)]} = \frac{C_0 V_{ref}^2}{4}$$

Otherwise, if $V_x > 0$, a downward correction will be operated, and as is discussed above, Fig. 3.3 shows the specific condition during this transition.

![Diagram](image)

Fig. 3.3 A downward correction in conventional SAR algorithm.

Thus, the power drawn from $V_{ref}$ should be

$$V_x(2) = -V_{in} + \frac{V_{ref}}{4}$$

$$E(1 \rightarrow 2) = -V_{ref} C_0[(V_x(2) - V_{ref}) - V_x(1)] = \frac{5C_0 V_{ref}^2}{4}$$
The power consumption $E(1\rightarrow2)$ in a downward correction includes two parts: the energy required to raise the voltage at node $V_x$, i.e. $E_{\text{node}} = -C_{\text{ref}}V_{\text{ref}}\Delta V_x = \frac{C_0V_{\text{ref}}^2}{4}$ and the energy required to charge the new capacitor ($C_1$) from GND to $V_{\text{ref}}$, i.e. $E_{\text{cap}} = C_0V_{\text{ref}}^2$.

### 3.2 Capacitor Splitting Technology

Now, considering capacitor splitting technology utilized in the modified capacitor array of this work (here, $C_2$ is split into $C_{2_1}$ and $C_{2_2}$), if there is a downward correction for the 2nd bit cycling, instead of connecting $C_1$ to $V_{\text{ref}}$ and returning $C_2$ (which does not exist here) back to GND, it is $C_{2_1}$ that needs to be connected to GND, which is shown in Fig. 3.4.

![Fig. 3.4 A downward correction in energy-efficiency algorithm.](image)

Thus, the power drawn from $V_{\text{ref}}$ is only required for charging the node $V_x$ and should be

$$E(1\rightarrow2) = E_{\text{node}} = -V_{\text{ref}}C_0(V_x(2) - V_x(1)) = \frac{C_0V_{\text{ref}}^2}{4}$$

In other words, compared with the downward correction in conventional SAR algorithm, no power is required for charging a capacitor from GND to $V_{\text{ref}}$ during the downward correction in this capacitor splitting structure.
On the other hand, an upward correction in this modified capacitor array is the same as that of conventional SAR algorithm, with a power consumption of $\frac{C_0 V^2}{4}$.

In conclusion, for one thing, the capacitor splitting technology (i.e. energy-efficiency algorithm) saves much energy during a downward correction since it avoids the extra but meaningless energy required for charging a capacitor from GND to $V_{\text{ref}}$, which is 4 times the energy needed for driving the change at node $V_x$. For another, the same power dissipation equal to $\frac{C_0 V^2}{4}$ for both upward and downward correction is realized thanks to the capacitor splitting structure.
CHAPTER 4: LAYOUT IMPLEMENTATION

4.1 Overview

Fig. 4.1 shows the complete layout implementation of the ADC, with marked red frames which respectively indicates different circuit blocks. Moreover, clear and enlarged circuitry without these frames, i.e. merely physical layout versions are given in Fig. 4.2 and Fig. 4.3, in the following 2 pages.

Meanwhile, important information about layout of the ADC is provided below in Table. 4.1.

<table>
<thead>
<tr>
<th>Fabrication Technology</th>
<th>IBM/Global Foundries 8HP, 130nm BiCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Size</td>
<td>944µm × 501µm</td>
</tr>
<tr>
<td>Metal Layer</td>
<td>M1, M2, M3, MQ, AM, LY</td>
</tr>
</tbody>
</table>

Table. 4.1 Layout information
Fig. 4.2 Layout of ADC
Fig. 4.3 Zoomed-in layout of latched comparator (CMP) and one of control logic modules in the whole ADC.
4.2 Latched Comparator

Recalling the principle of the latched comparator discussed in Section 2.2, especially the schematic shown in Fig. 2.2, it is obvious that the layout of this circuit must be very symmetric for both sides of the input transistors (N1 and N2), as well as the pair of back-to-back inverters and associated pull-up transistors (P1 and P2). Otherwise, different layout structure may boost the environment or process variation for the response of the circuit and eventually lead to wrong comparisons. Therefore, the symmetric layout of the latched comparator is implemented as shown in Fig. 4.4.

![Fig. 4.4 Layout of latched comparator (CMP).](image)

4.3 Differential Binary-weighted Capacitor Array

First take a look at Fig. 4.5 in the next page, the final layout implementation of the positive binary-weighted capacitor array. In order to present a clear figure of the layout
with much bigger patterns, as well as to make the discussion more concise, the negative capacitor array, which is almost the same, is omitted here.

As the accuracy of charge redistribution ADC is mainly based on the accuracy of the capacitor array, instead of directly choosing capacitors with binary-weighted capacitance along the array, the binary-weighted value of a capacitor is achieved more accurately by using binary-weighted numbers of unit capacitors (40fF in this work) to constitute the corresponding capacitor. As a matter of fact, all those identical square capacitors in Fig. 4.5 are just numerous unit capacitors mentioned above.
On the other hand, parasitic capacitance at the input node of the comparator is a main cause accounting for inaccuracy. As far as MIM capacitors are concerned, top plates (AM layer, dark blue) have smaller parasitic capacitance, thus top plates are all connected to the input node of the comparator while bottom plates (LY layer, yellow) are connected to logic control modules. As is shown in Fig. 4.5, AM layer goes vertically along all the capacitors and finally converges on the upper and lower side of the array, while different wires in LY layer only connects some capacitors together to constitute the specific capacitors.

---

**Fig. 4.6 Layout illustration of the capacitor array (for both positive and negative arrays).**
Actually, parasitic capacitance is also significantly introduced by the wiring interconnection and other circuit elements adjacent to the capacitor array. Therefore, one way to help avoid this is by designing a circle of dummy capacitors around the effective capacitor array, which is shown in Fig. 4.6 in the previous page.

Under this circumstance, since the capacitors originally forming the edges of the array are no longer located at the edge (now dummy capacitors forms the edge), every unit capacitor in the effective capacitor array should have identical surroundings (i.e. each unit capacitor is surrounded by eight unit capacitors). In other words, the equivalent parasitic capacitance of every unit capacitor is approximately the same. Consequently, it will still satisfy the requirement of binary-weighted capacitance in the charge redistribution structure. In addition, common-centroid layout is implemented to help tolerate process deviation. The above discussion can be illustrated by Fig. 4.6, where the number representation for these binary-weighted capacitors corresponds with the capacitor names (and also the multiples of unit capacitor) in the schematic of capacitor array shown in Fig. 2.3, and DM means dummy capacitors.

Fig. 4.7 in the next page shows the connection of the capacitor array with logic control modules using highlight wirings. Different colors indicate the constitution of larger binary-weighted capacitors, which exactly follows the common-centroid layout depicted by Fig. 4.6.
4.3 Registers Utilized in Control Logic Module, State Machine and Shift Registers

Register is a key component in control logic module, state machine and shift registers, and therefore, the layout of register should be carefully designed as a common cell appropriate for all of the above structures.

As is shown in Fig. 4.8 in the next page, the layout outline of register is a rectangle, which can be easily connected to other registers (to constitute state machine or shift registers) without wasting area because they are all rectangles. The middle wire (M2
layer) is VDD while the upper and lower wire is GND, which also helps alleviate the complex wiring when connecting registers in series, since they may share the same middle wire as VDD and the upper and lower wire as GND. The position of input D and output Q/Qbar is also designed for interconnection considerations.

Fig. 4.8 Layout of register.

4.4 Control Logic Module

Fig. 4.9 shows the layout of the logic circuit controlling C128+ and C128-, which connects C128+ and C128- with Vs or GND respectively, according to the comparison result from Bit Cycling 0.

Fig. 4.9 Layout of the logic circuit controlling C128+ and C128-.
Similarly, Fig. 4.10 shows the layout of the logic circuit for C32 – C1, where double transmission gates used as switches are implemented.

![Fig. 4.10 Layout of the logic circuit controlling C32 – C1.](image)

### 4.5 Other Considerations

In order to avoid clock deviation, the clock distribution follows the pattern of “H” Tree.

Analog modules are placed away from pure digital circuits and massive substrate contacts are placed to help decouple noise caused by clock edges.
CHAPTER 5: SIMULATION RESULTS

5.1 ADC Functionality Verification

Fig. 5.1 shows the circuit used for simulation.

Chapter 3 has taken $V_{in} = 820\text{mV}$ as an example to show how the circuit works and finally proves the validity of the proposed ADC. Moreover, a simulation result acquired from QRC model of layout is given in Fig. 5.2.
In addition, 2 more conditions are simulated, i.e. Vin = 62mV and Vin = 550mV. Thus, small input voltage (e.g. 62mV) and medium input voltage (e.g. 550mV), as well as large input voltage (e.g. 820mV) can all be tested, to verify the functionality and linearity of the ADC in this work.

### 5.2 Power Consumption

Simulation for power consumption is done for Vin = 62mV and Vin = 820mV, at a conversion rate of 55.5-kS/s (i.e. a clock frequency of 500kHz).

![Current waveform of power supply VDD](image)

Fig. 5.3 The current waveform of the power supply VDD (for Vin = 62mV).

Fig. 5.3 shows the current waveform of the power supply VDD, for Vin = 62mV. By using Cadence calculator, the average current during a complete conversion (9 clock cycles) can be got, i.e.

\[ I_{av} = 11.63 \mu A \]

Consequently,
\[ P_{av} = VDD \cdot I_{av} = 1V \cdot (11.63\mu A) = 11.63\mu W \]

which is satisfied with the power consumption requirements, thanks to the energy-saving capacitor array and latched comparator that has no static power dissipation.

Fig. 5.4 shows the current waveform of the power supply VDD, for Vin = 820mV.

By using Cadence calculator, the average current during a complete conversion (9 clock cycles) can be got, i.e.

\[ I_{av} = 11.6\mu A \]

Consequently,

\[ P_{av} = VDD \cdot I_{av} = 1V \cdot (11.6\mu A) = 11.6\mu W \]

which is satisfied with the power consumption requirements, thanks to the energy-saving capacitor array and latched comparator that has no static power dissipation.

In conclusion, for different input voltages, the power consumption may have a small difference mainly due to the various situations of charging on the capacitor array, but in
general, the power consumption is just within the range of 11 – 12\(\mu\)W and thereby is quite suitable for the required low-power application.
CHAPTER 6: CONCLUSION

Reviewing the wide focus of neuron signals and neural recorder chips, the work aims at realizing a low power ADC that is suitable for neural recorder applications.

Owing to the design of a dynamic latched comparator which has no static power dissipation and applying the methodology of capacitor splitting in the modified capacitor array with related switching logic sequence to achieve power efficiency, a 1-V 8-bit 55.5-kS/s ultra-low power (typically less than 12-µW) SAD-ADC intended for neural recorder applications is realized based on IBM/Global Foundries 8HP 130nm BiCMOS technology.

Schematic and layout simulations are done respectively to verify the functionality, linearity and power consumption of the proposed ADC.

Considering that most portable low power biomedical applications have sensors sampling analog biological signals and demand an A/D conversion to acquire digitized signals that can be further processed by subsequent digital modules, the low power ADC presented by this work may also be well-suited.

In addition to realizing the clock generator on chip, future work can be done concerning the optimization of chip layout to help reduce parasitic parameters and avoid inaccurate sampled voltage at the input node. Thus, conversion errors can be prevented more sufficiently. Using standard cells for the digital modules shall improve the performance as well. Moreover, the ADC may be fabricated at last, and therefore the real chip can be verified practically.
BIBLIOGRAPHY

