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Design of a 10GHz RF power amplifier in 130nm CMOS technology based on Wilkinson combiner methodology

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DESIGN OF A 10GHZ RF POWER AMPLIFIER IN 130NM CMOS TECHNOLOGY BASED ON WILKINSON COMBINER METHODOLOGY

by

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I would like to dedicate this work to my beloved parents and friends, for their unconditional love, patience and support.

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I would like to show my deepest acknowledgment and respect of Professor Ronald W. Knepper, my erudite advisor, who guides me in discovery of RF/Analog IC design and helps me get over countless difficulties and challenges during the realization of my thesis.

DESIGN OF A 10GHZ RF POWER AMPLIFIER IN 130NM CMOS TECHNOLOGY BASED ON WILKINSON COMBINER METHODOLOGY

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ABSTRACT

There is a growing demand today to design and fabricate RF power amplifiers at high frequencies above 5GHz that can directly drive a 50Ω antenna with sufficiently high transmission power to meet the needs of various wireless communication applications. This has typically been done by using GaN or other III-V technologies to build the power amplifier transistor, in order to allow for the use of much higher power supply voltages, than are used in today's silicon technologies. For example, a 5W GaN power amplifier at 5GHz would typically make use of a VDD of 5V to 10V, and would be done as a discrete device on a separate module from the RF analog circuitry built out of silicon. With the continuing evolution of Moore's Law, silicon technologies in use today for high frequency wireless communications typically are using VDD of 1.5V or less.

There is a desire, however, in many wireless applications to be able to place the RF power amplifier on the same silicon chip as all the other RF/analog IC circuitry, in order to save chip fabrication cost. Consequently, research in improved methods of RF power amplifier design in silicon technology is being done in many IC design laboratories in order to increase the RF power output of power amplifiers built in silicon. This MS Thesis proposes the complete design of a four channel RF power amplifier by using the Wilkinson combiner with 27dBm output power. All the circuits are designed and implemented based on the Global Foundries 130nm SiGe BiCMOS

technology and design kit at a frequency of 10GHz with a VDD = 1.5V, to provide 0.5W of RF output signal power into a 50Ω antenna.

Contents

List of Tables

List of Figures

List of Abbreviations

BPF	.....	band-pass filter
CMOS	.....	Complementary Metal-Oxide-Semiconductor
DPA	.....	digital power amplifier
GPS	.....	the Global Positioning System
HP	.....	Hewlett-Packard
ICs	.....	Integrated Circuits
LNA	.....	Low Noise Amplifier
LNTA	.....	low-noise transconductance amplifier
LO	.....	local oscillator
LPF	.....	low pass filter
PAE	.....	Power Added Efficiency
PTFE	.....	Polytetrafluoroethylene
RF	.....	Radio Frequency
SC	.....	switched-cap circuit
SoC	.....	System on Chip
VCO	.....	Voltage Control Oscillation

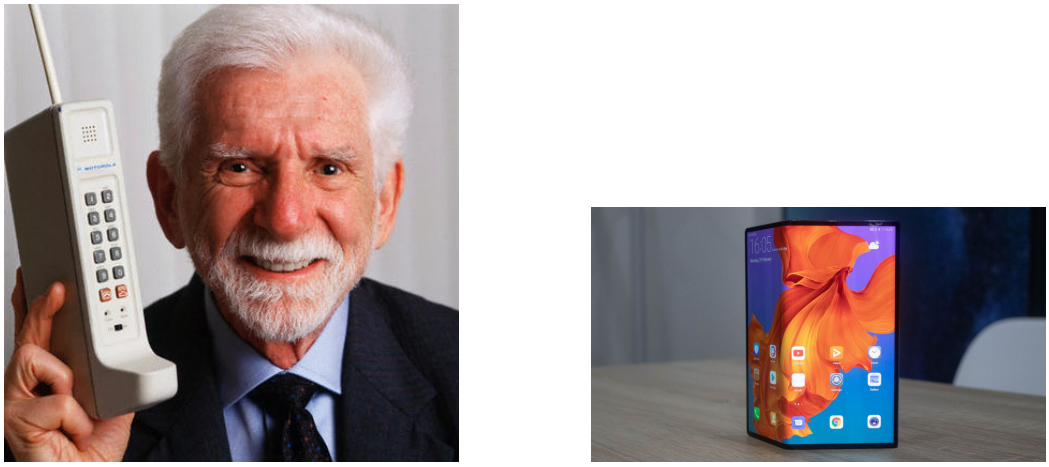
Chapter 1

Introduction

There has been significant growth in the field of RF communication over the past four decades. For instance the mobile phone industry, in 1973 when the first hand-held mobile phone was demonstrated by Mr.Martin Cooper of Motorola, it weighted around 1-Kg with no longer than 35 minutes talk time Figure 1·1. By the end of 1978, AT&T's first cellular phone network in Chicago served about 1,300 customers. From Figure 1·2, we can see, with over 4.7 billion (Statista 2019) wireless phone subscribers worldwide, our cell phones serve as an encyclopedia, a shopping terminus, a GPS guide, a multimedia center, and lastly a telephone. With the continuing growth and success of the wireless communications market, it can be envisioned that in the near future, every home device and appliance, such as ovens, TVs, laptops, etc., will eventually be connected into one wireless network–all thanks to the enormous development of global wireless communications technology(Boccuzzi, 1995).

With the development of wireless communications technology, it requires higher level integration in hardware design for higher volume applications to meet lower cost, lower power consumption and better performance. The main goal in designing wireless transceivers is to merge both digital and analog circuits as many as possible on a single silicon chip in an economical way. Hence the Complementary Metal-Oxide-Semiconductor(CMOS) was first invented purely for digital Integrated Circuits(ICs), yet due to its predominant position in IC world, more and more analog/Radio Frequency (RF) modules such as Operational Amplifiers (Op-Amps), Low Noise Am-

plifiers (LNAs), etc. are widely used. In the past several decades, the minimum feature size of CMOS technology has fallen from 500-nm to 7-nm as characterized by the Moores Law, which basically says that the information storage capacity of a silicon chip, as well as its information processing power, grows exponentially with time. Although there are various challenges in continuing this progress, it is believed that CMOS technology will still dominate both digital and analog IC market in the foreseeable future, and probably be the only way at present time to realize an entire system on a single die(El-Desouki et al., 2005).



(a) (b)

Figure 1·1: (a)Martin Cooper and his first handheld mobile phone (b)One of the smartest phone

1.1 Research Motivation

Figure 1·3 shows both conventional analog-intensive RF transceiver and digital-intensive RF transceiver. For both RF transceiver, Power Amplifier plays an important role. However, Power Amplifiers (PAs) probably are the last module that has not been widely and fully integrated on silicon. Nevertheless, because of the low cost and the potential for high-density and functionality, CMOS has long become an attrac-

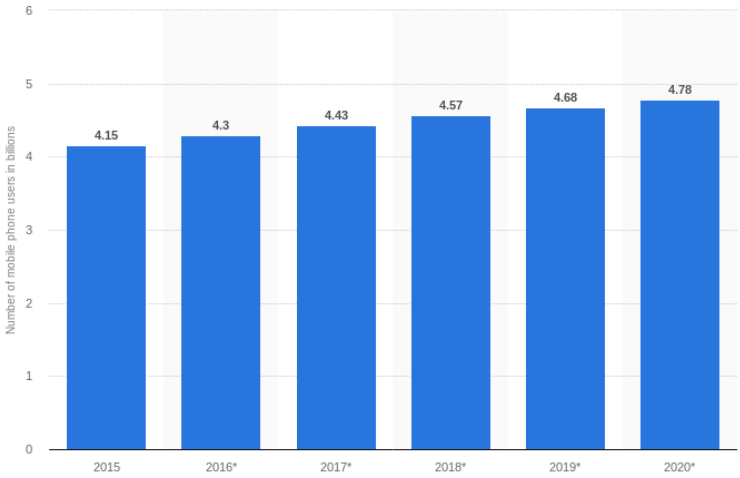


Figure 1·2: Number of mobile phone users worldwide from 2015 to 2020 (in billions)

tive technology for RF power amplification. In 1997, David Su and his colleagues in Hewlett-Packard (HP) reported the first CMOS RF PA which could provide 1-W of output power from a single 2.5-V DC supply to a 50Ω load(Kuo and Lusignan, 2001). The amplifier prototype was fabricated in a standard 0.8-um CMOS technology with a working frequency in the range of 824-MHz to 849-MHz, Power Added Efficiency (PAE) of 42%, and drain efficiency of 62%. Although this PA was built not suitable for full integration, for the first time, the design demonstrated the ability of CMOS technology of providing efficient RF signal power amplification at 800-900MHz in low-voltage applications(Papananos and Koutsoyannopoulos, 1998).

Ever since then, there have been quite a few publications on CMOS RF PAs. However, same as(Kuo and Lusignan, 2001), the major hurdle that prevents them from being fully integrated in one chip is their impedance transformation networks which require off-chip components such as inductors, capacitors, or bond-wires. Driven by the demands from marketing, great efforts have been contributed to the design of low-loss, fully integrated, on-chip impedance transformation networks(Liu and Wang,

2006). Soon after,there are more chance for designers to integrate their circuits on silicon because of inductors, which can take place of transformers. So there are wide applications in many circuits. The intrinsic merits of DC isolation and voltage step-up have made them very promising candidates in todays PA impedance transformation network designs. We will revisit this part of work later in this section(Beyerstedt et al., 2018).

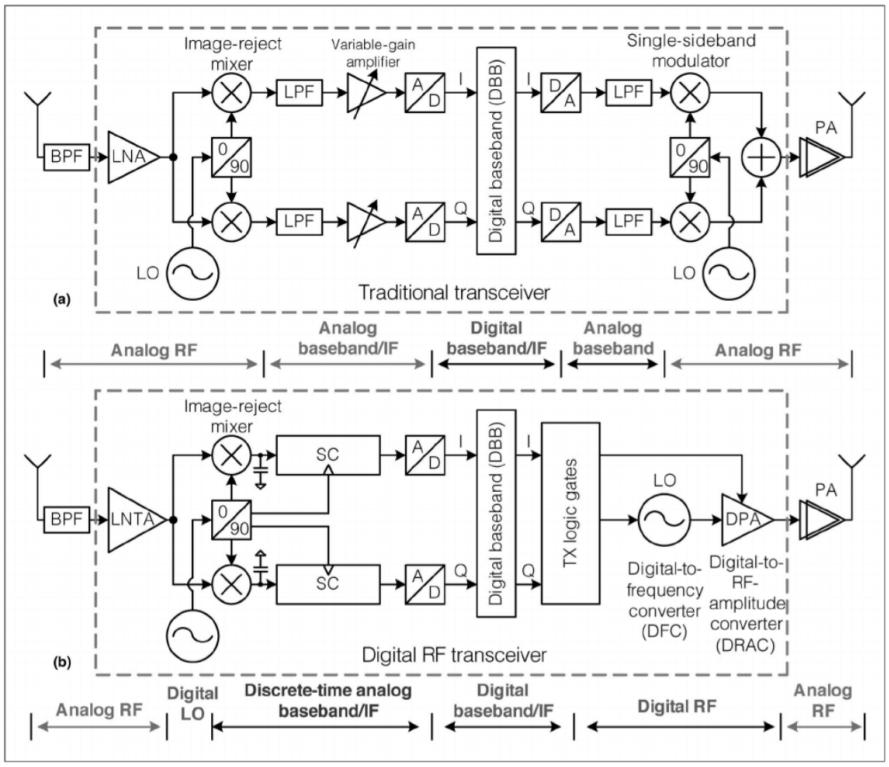


Figure 1·3: (a) conventional analog-intensive RF transceivers and (b) digitally intensive RF transceivers. (BPF: band-pass filter); DPA: digital power amplifier; I: in-phase signal; IF: intermediate frequency; LNA: low-noise amplifier; LNTA: low-noise transconductance amplifier; LO: local oscillator; LPF: low-pass filter; PA: power amplifier; Q: quadrature signal; SC: switched-cap circuit.)

Besides integration, there is another serious issue associated with PA design which is inherent to conventional PA(Razavi, 2006). It is well known that a PA can only

achieve maximum efficiency at peak output power. As output power decreases, efficiency drops rapidly. However, the need to conserve battery power and to mitigate interference to other users necessitates the transmission of power levels well below the peak output power of the transmitter. Moreover, since spectrum is a scarce commodity, modern transmitters for wireless communications employ spectrally efficient digital modulations with time varying envelope. Because of these reasons, the PA transmits much lower than peak output power under typical operating conditions(Javidan and Atarodi, 2011).

This thesis is to design a 10GHz high efficiency 500mW (27dBm) Power Amplifier in 130nm CMOS-technology. The power added efficiency should be 20% and the gain around 66dB. The approach used is first to study and simulate seven different types of promising amplifier topology, and then decide which one is the most promising to take further to a genuine design.

The goal of this thesis was to make both circuit design and layout design, which fulfills the given requirements. The output power should be more than 500mW with good efficiency.

1.2 Research Objective

To date, there has been relatively little research on the design of a CMOS PA targeting good average efficiency. This work proposes a power combining transformer to address this issue. This transformer provides measures for simple yet elegant power control and average efficiency enhancement by modulating the RF load. The control could be implemented using digital approaches or analog approaches. Average efficiency enhancement with digital control was successfully demonstrated with a fully integrated CMOS PA (Javidan and Atarodi, 2011).

Because of the high output power and high frequency requirement, this thesis uses

several pre-drivers for this power amplifier. As the output power should be more than 500mW, this work utilized four channels power amplifier then using a LC balun to combine all four channels to one channel to achieve the high output power goal.

With 1.5V supply, this design transmits 26.98dBm (500mW) output power. To the authors knowledge, this is the first reported fully integrated CMOS power amplifier with 4-to-1 lumped Wilkinson combiner which achieve over 500mW output power based on 130nm CMOS techonology from Cadence 8HP schematic simulation.

1.3 Thesis Organization

Chapter 2 has three main parts. First part presents an overview of power amplifier, introducing seven different types of power amplifiers and metrics to evaluate power amplifiers performance. Second part introduces different ways to achieve power combination. The last part introduces some important factors in designing power amplifier. Chapter 3 starts talking about a detailed description of design process of schematic. Chapter 4 presents the layout design of each module from the schematic view. Chapter 5 shows the simulation results of this thesis. At last, Chapter 6 concludes this work and gives some suggestion for future research.

Chapter 2

Previous Work

This chapter introduced some previous work related to power amplifier and Wilkinson combiner, then it also includes several vital factors in this thesis design.

2.1 Power Amplifier Classification

There is more than one way to classify power amplifiers. A common way is to label each type of power amplifier with roman letters such as A, B, AB, C, D, E, F, etc. This is done according to either the biasing points or passive components in the output network which helps to form the drain voltage and current into a certain shape. These power amplifiers can be classified as either linear amplifiers or non-linear amplifiers. The class A, class B, and class AB are normally categorized as linear amplifiers as opposed to the class C, class D, class E, and class F that are labeled nonlinear amplifiers. A brief introduction to each class of PA is shown below(Burghartz, 2013).

2.1.1 Class A Power Amplifier

A class A amplifier shown in Figure 2·1 is a common linear amplifier. It is biased in such a way that the active device of the amplifier conducts throughout the entire cycle. Therefore, the main advantage of the class A amplifier is that it has very good linearity. However, the disadvantage is its low efficiency which is ideally only about 30%(Lee, 2004).

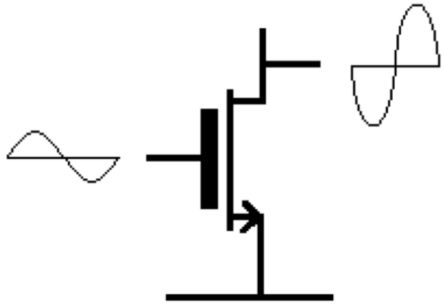


Figure 2·1: Class A Power Amplifier

2.1.2 Class B Power Amplifier

The class B is more efficient than the class A, about 50% , but has issues with linearity at the crossover point where one device turns off and the other device is turning on and vice versa(Lee, 2004). As shown in Figure 2·2

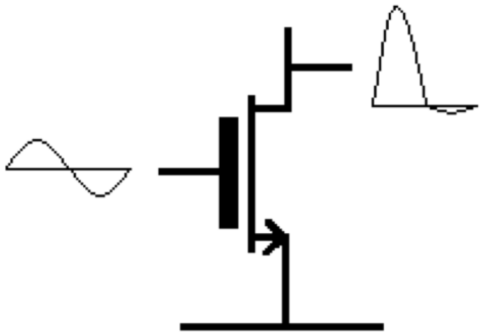


Figure 2·2: Class B Power Amplifier

2.1.3 Class AB Power Amplifier

One kind of class AB amplifier is considered a linear amplifier shown in Figure 2·3. The class AB is a combination of the class A and the class B amplifiers. The major difference between the class AB and the class B is that the class AB allows two

devices to be on at the same time near crossover but for a very short amount of time. Therefore, each device conducts for more than half a cycle but less than a full cycle. Because of this, better linearity and efficiency are both achieved at a balanced point. The linearity of the class AB is better than the class B, and the efficiency of the class AB is higher than the class A(Lee, 2004).

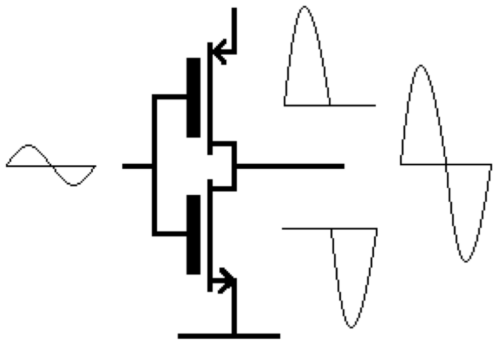


Figure 2·3: Class AB Power Amplifier

2.1.4 Class C Power Amplifier

A class C amplifier is shown in Figure 2·4. The active device is biased in a way that the device only conducts less than half cycle of the input signal. According to (Montaseri et al., 2018), the class C amplifier can reach an efficiency of 85% theoretically. However, the class C amplifiers do not have good linearity. The class C amplifier is not suitable for audio amplifiers due to its high distortion. Therefore, they are normally used for high power output applications at RF frequencies and distortion due to higher harmonics can be filtered out(Lee, 2004).

2.1.5 Class D Power Amplifier

A class D amplifier, shown in Figure 2·5, is considered to be a switching, or PWM, amplifier. It is commonly used as an audio amplifier. Compared to linear amplifiers,

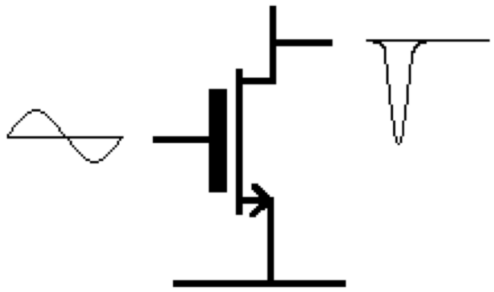


Figure 2·4: Class C Power Amplifier

the power loss in the class D amplifiers can be significantly less because the active device MH or ML is either fully on or off. The transistors, MH and ML, cannot be turned on at the same time. When MH or ML is fully on, there is no power dissipation ideally in the switching active devices due to no path from the power supply to ground when one of the transistors is fully off. Therefore, efficiency can possibly be as high as 90% to 95% theoretically. Normally a PWM carrier signal that is driving output devices is modulated by an audio signal. A low pass filter can be placed in the output stage to remove the high frequency components of the PWM signal(Lee, 2004).

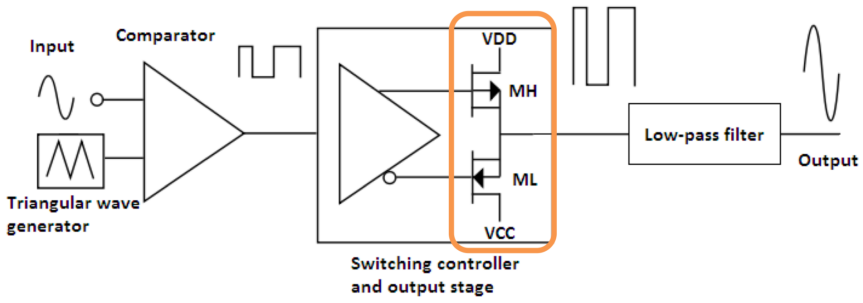


Figure 2·5: Class D Power Amplifier

2.1.6 Class E Power Amplifier

A class E power amplifier shown in Figure 2·6 is considered a nonlinear or switching amplifier. The distinctive feature of the class E is that the drain voltage and current of the switching device are created in such a way that they do not occur simultaneously. This results in less power consumption. Therefore, the theoretical efficiency is very high. The class E is a popular choice for RF PA designs when compared to other options. More analysis on the class E amplifier will be discussed in the later chapters(Lee, 2004).

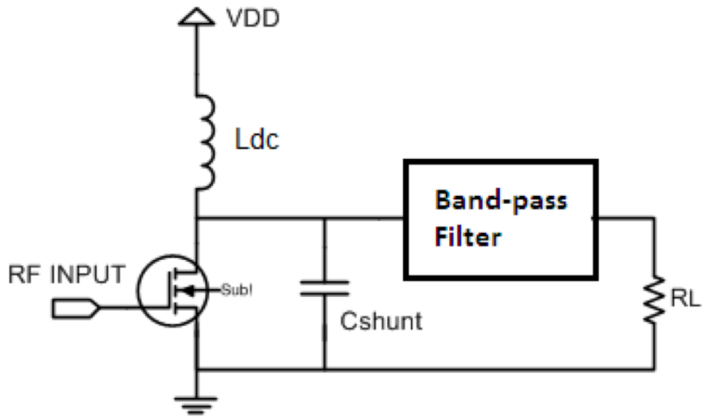


Figure 2·6: Class E Power Amplifier

2.1.7 Class F Power Amplifier

A class F amplifier shown in Figure 2·7 is another type of switching mode amplifier which is nonlinear. Just like the class E amplifier, the class F is a switching amplifier with a unique output network that shapes the drain voltage and current so that they do not overlap each other which reduces power dissipation. Compared to the class E PA, the major difference is in the output network. The class F PA includes two parallel LC resonant tanks. One tank serves as a matching network tuned at the

fundamental frequency. The other tank is a harmonic tuning network tuned at the 3rd order harmonic. Therefore, a short circuit can be seen at the even order harmonics, and an open circuit at the 3rd order harmonic. By doing so, ideally a square wave drain voltage and a half bridge rectified sine wave drain current are created but do not overlap each other for less power dissipation(Lee, 2004) .

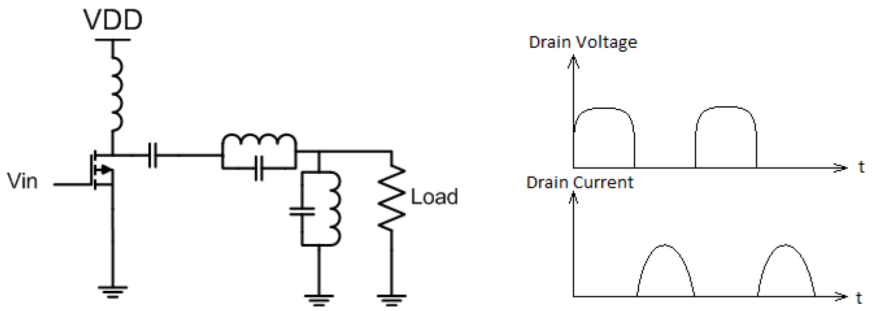


Figure 2·7: Class F Power Amplifier

Both linear and non-linear power amplifiers have positives and negatives. On one hand, the linear power amplifiers generally have good linearity but poor efficiency. On the other hand, the nonlinear power amplifiers generally have good efficiency but have poor linearity. So a trade-off between linearity and efficiency becomes a major factor for choosing an appropriate power amplifier.

Linearity of amplifiers refers to how an output signal is precisely proportional to an input signal of an amplifier while the signal power is amplified. The purpose of having high linearity is to make sure the content in the signal is not altered while the signal is amplified. For linear amplifiers like class A, its output signal is precisely proportional to its input signal since the active device conducts throughout a full cycle of sine wave. The down side of the linear amplifiers is low efficiency. The class A amplifier is an example of this because the current drawn from power supply flows through the active device throughout the full cycle of sine wave so the power efficiency

is much lower compared to non-linear amplifiers(Rostomyan et al., 2018).

Efficiency, or power efficiency of an amplifier, is used to evaluate how well the amplifier transfers the DC power from the supply into useful AC output power without wasting it. One advantage of non-linear power amplifiers like the class E PA is their higher efficiency because the conducting angle or time for nonlinear amplifiers is much less than linear amplifiers in a cycle of a sine wave. Therefore, there is less current drawn to ground through active devices as opposed to current delivered to the output, which is good for efficiency. However, one negative about non-linear amplifiers is poor linearity. The output waveform is distorted compared to the input waveform in the process of power amplification. In Table 2.1, a comparison of the theoretical efficiency and linearity among the discussed power amplifier types is presented.

Table 2.1: Comparison in Efficiency Among Different Amplifier Classes

class	*operation*	*Theoretical Efficiency*
A	Linear	50% max
B	Linear	78.5% max
AB	Linear	50%-78.5%
C	Non-linear	85%
D	Non-linear	90%or100%
E	Non-linear	100%
F	Non-linear	88.4%

To choose an appropriate power amplifier requires considerations on signal modulation scheme, major performance parameters, and other factors for the benefits of this design project.

2.2 Wilkinson Combiner

Wilkinson type combiner/splitter(Wentzel et al., 2006) is found as a good choice for development of the input splitter and output combiner for power amplifier. Wilkinson combiner/splitter is a 3 port (in2×2 scheme) lossy, matched and reciprocal network. Figure 2·8 shows the scheme of a 2×2 Wilkinson combiner/splitter. Port 3 of

characteristic impedance Z_0 is split in two arms with each arm having a quarter wave ($\lambda/4$) impedance transformer of characteristic impedance . Port 1 and 2 are connected at the other end of transformer. Isolation between the port 1 and 2 is achieved by connecting a resistor of $2Z_0$ between the two ports.

For characteristic impedance Z_0= 50ohm and design frequency f_0 = 10GHz Quarter wave transformer characteristic impedance is $Z_{trans} = \sqrt{2}times50 = 70.7\Omega$ The length of transformer is $L_{trans} = \frac{\lambda_0}{4\times\sqrt{\varepsilon_r}}$, where ε_r is PTFE dielectric constant.(Wilkinson, 1960)

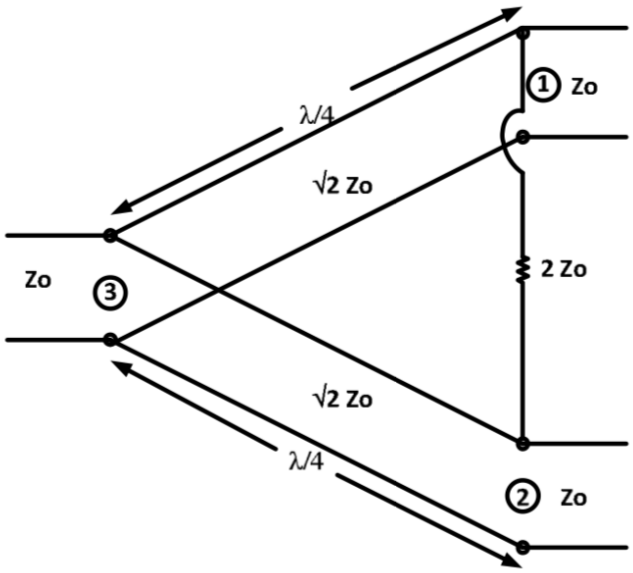


Figure 2·8: Traditional Wilkinson Combiner

2.3 Important Parameters

2.3.1 Terms of Efficiency

Drain Efficiency

The drain efficiency is defined as the relationship between the fundamental output power and the required dc-power: $\eta_d = \frac{P_{out,fc}}{P_{DC}}$

PAE-Power Added Efficiency

An often used measure of efficiency is the Power Added Efficiency (PAE) defined as:

$$PAE = \frac{P_{out,fc} - P_{in,fc}}{P_{DC}} = \eta_d(1 - \frac{1}{G})$$

Some will argue that this efficiency measurement is the most correct one (in comparison with the drain efficiency) because it takes the input power into account. The drawback is that the PAE can become negative for gain levels below one (output power less than input power).

Power Gain

The power gain is defined as the ratio between the output and input power at the fundamental frequency: $G = \frac{P_{out,fc}}{P_{in,fc}}$

Stability

Stability is a very important element to consider when designing a power amplifier. Because of the high gain, oscillations are bound to happen if this is not considered.

The most used measurement of stability is the Rollets stability factor, often called the Kfactor. If this K-factor is greater than one (and $\Delta < 1$, as defined below), it means that the amplifier is unconditionally stable. That an amplifier is unconditionally stable means that it is stable for all possible input and output impedances that can be found within the Smith-chart (from the center to the perimeter (gamma=1) at any phase angles). Conditionally stable would on the other hand be an amplifier that is stable when the input and output sees the intended impedances (often 50Ω), but could be unstable when mismatched(Lee, 2004).

The K-factor does not reveal anything about how unconditionally stable the amplifier is. In other words an amplifier with K-factor of 100 can be closer to oscillations

than one with K-factor of one. The μ-factor (mju-factor) is a better measurement for making comparisons like this, but since this factor is not included in Cadence, the K-factor is used in this thesis.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{21}S_{12}|}$$

Another measure of stability is stability circles. These are drawn in the Smith-chart. This measure can for instance be used for conditionally stable amplifiers. The amplifier will be stable in the area between the circle and the rest of the smith-chart on the side which contains the center of the smith-chart. In this design, most matching is based on smitch chart.

S-parameters

S-parameters (scattering parameters) are being used to describe the behavior of RF-circuits. They are intended to be used for linear systems, small signal analysis. Gain, stability, voltage standing wave ratio, reflection coefficients and return loss can all be described by S-parameters. The S-parameters are easily described by means of a two-port network like the one shown in Figure 2·9. a1 is the incident and b1 is the reflected voltage wave at port 1 a2 is the incident and b2 is the reflected voltage wave of port 2. The S-parameters are defined as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

This means that the reflected voltage wave, b1, consist of the reflected part of the incident voltage wave, a1, plus the backward amplified part of the incident voltage wave at port 2, a2. S11 is the input port voltage reflection coefficient, and S21 is the forward voltage gain. They are equal to :$S_{11} = \frac{b_1}{a_1} Q = \frac{2\pi f L}{R_s}$,$S_{21} = \frac{b_2}{a_2}$. When port 2 is terminated in the systems impedance Z_0, then a_1=0. S22 is the output port

voltage reflection coefficient, and S12 is the reverse voltage gain. They are equal to : $S_{22} = \frac{b_2}{a_2}$,$S_{12} = \frac{b_1}{a_2}$. When port 1 is terminated in the systems impedance Z_0, then a_1=0.

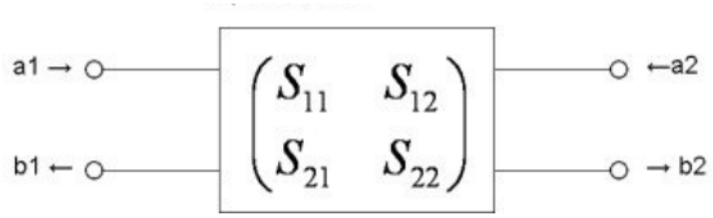


Figure 2·9: Quality Factor(Q-factor)

The quality factor of an inductance is defined as : $Q = \frac{2\pi fL}{R_s}$,Where R_s is the resistance of the non-ideal inductance. The Q-factor is a measure method of how much power loss the inductance contributes to. A high Q-factor means that the inductance contributes to a small loss. As one can see from the previous equation, an inductance with a constant Q-factor will contribute to more loss if the frequency increases. When making a realistic circuit design it is important to consider that an inductance will never be lossless. There is loss due to the quality factor, and there is loss due to the DC-resistance. If the current through the inductor consists only of a given frequency, the inductance is easy to model by simply including a series resistance with the value given by $Q = \frac{2\pi fL}{R_s}$. One can also model this resistance as a shunt resistance. Then the value is given by : $R_{shunt} = (1+Q^2)\times R_s$ If we however have both DC-current and RF-current, we need more realistic models, which as showed in Figure 2·10. In Figure 2·10, the DC-loss is included in the R_{DC} resistance, while the RF-loss from the non-infinite Q-factor is included via R_p . R_p is the shunt version of R_s which is calculated as follows : $R_p = (1 + Q^2) \times (R_s - R_{DC})$

In Figure 2·10, the DC-path and the RF-path are separated by a large inductance, $L_{RFblock}$ so that the RF-current sees the intended R_s-resistance, and the DC-current

sees the R_s resistance (here it is assumed that the resistance is larger than the R_{DC}-resistance). (Cripps, 1999)

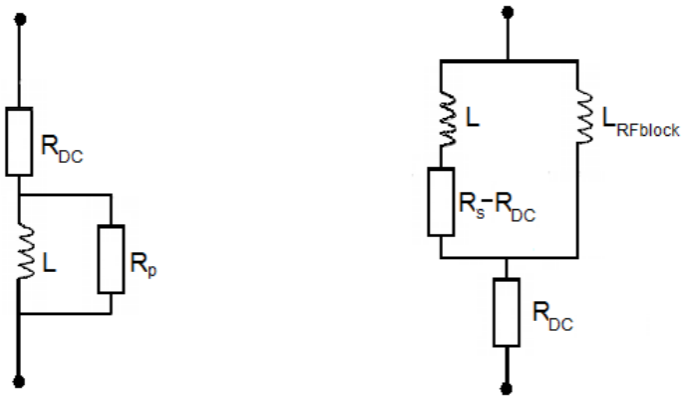


Figure 2·10: DC-current and RF-current

2.3.2 Impedance Matching

Impedance matching is the practice of designing the input impedance of an electrical load or the output impedance of its corresponding signal source to maximize the power transfer or minimize signal reflection from the load. Firgure 2·11 shows the impedance transformation network. (a) presents an L-match network and (b) presents an L-match network with inductor loss. The power transference will reach the maximum when the input impedance of the amplifier is the complex conjugated to the source impedance, and the output impedance is complex conjugated to the load impedance.

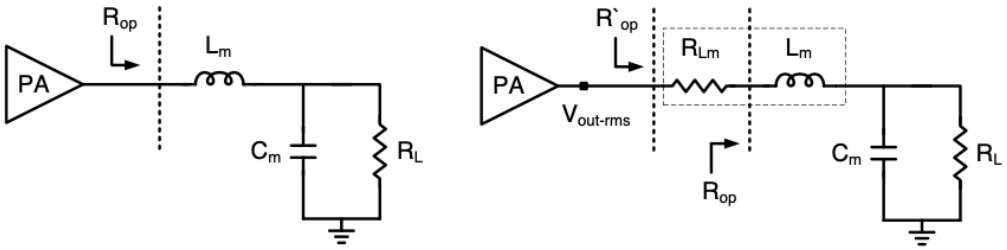


Figure 2·11: Impedance transformation network: (a) an L-match network and (b) an L-match network with inductor loss.

Chapter 3

Schematic Design

3.1 Design Procedures

The design process of the RF power amplifier is presented in the flow chart in Figure 3.1. From the beginning, it is important to be clear in the design specification and aim of the design, which is helpful in achieving a successful design.

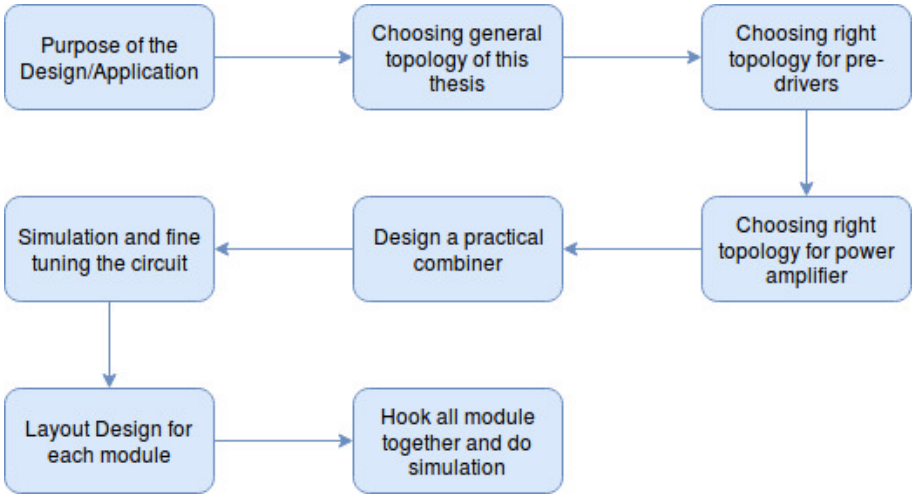


Figure 3·1: Thesis Design Flow

Here is a list of design specifications that were known before designing the circuitry. This design is based on the following values.

- Power Supply: 1.5V
- Operating Frequency: 10GHz

- Input RF amplitude: 10mV
- Input Impedance: 100Ω
- Output Impedance: 50Ω

3.2 Suitable Topology

As mentioned before, this thesis is aimed to design a power amplifier module with 1W output power with 50ohm load antenna. This means the final stage output RF voltage should be 10V at the peak. In considering the gain of power amplifier is limited by DC supply voltage, so I use two pre-drivers to provide 1V input signal for power amplifier module. Each pre-driver should have voltage gain of 20dB, which means the first stage pre-driver can amplify 10mV input signal to 100mV output signal for the second stage pre-driver. Then the second pre-driver drives the 100mV signal to 1V for power amplifier. Even by using two stages pre-drivers, it is still hard to achieve high enough output power. It probably needs four channels to realize this goal. Then I use a 4-to-1 lumped Wilkinson combiner to combine the same four channels to single one end output. The proposed single channel is shown as Figure 3·2 and four channels are shown as Figure 3·3

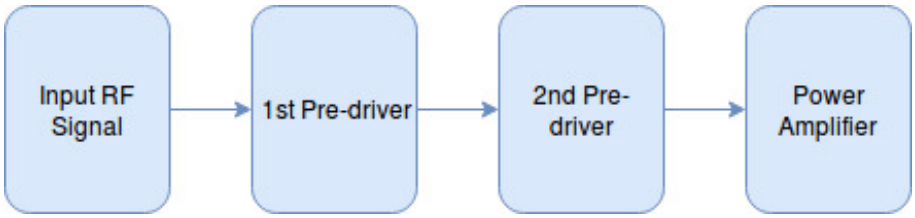


Figure 3·2: Single Channel Power Amplifier

Figure 3·3: Four Channels Power Amplifier

3.3 Circuit Design

3.3.1 First Pre-driver Design

For the first pre-driver, I choose cascode structure as the basic structure as this structure can provide higher voltage gain, which is widely used in analog circuit design. Cascode structure is consisted of one common source stage and one common gate stage. Figure 3·4 (a) shows the common source amplifier and Figure 3·4 (b) shows the common gate amplifier.

(a) (b)

Figure 3·4: (a)Common Source Amplifier (b)Common Gate Amplifier

By considering the Millers theorem, the cascode amplifier can be converted to the equivalent small signal model as shown in Figure 3·6, after combining C_{gs1} and the value coming from C_{gd1}, the C_{Gs1} presents the new value. Y_{ds1} is the combination value of g_{ds1}, C_{ds1} and the value coming from C_{gd1}.

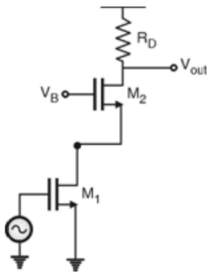


Figure 3·5: Cascode Amplifier

According to the small signal model of cascode amplifier, the voltage gain can be calculated as: (Bu et al., 2011)

$$A_v = \frac{-g_{m1}}{Y_L + \frac{Y_{ds1}(Y_L+Y_{ds2})(1-\omega^2 L_{TL}C_{gs2})+j\omega C_{gs2}(Y_L+Y_{ds2})}{g_{m2}+Y_{ds2}(1-\omega^2 L_n C_{gs2})}}$$

After calculating the voltage gain as 20dB, this thesis chose one stage cascode amplifier at the first time. Because the input impedance is 100Ω and the output impedance is 50Ω, the gain needs to be increased by 3dB. Taking this factor into consideration, this thesis choose to design a two-stage amplifier for the first pre-driver.

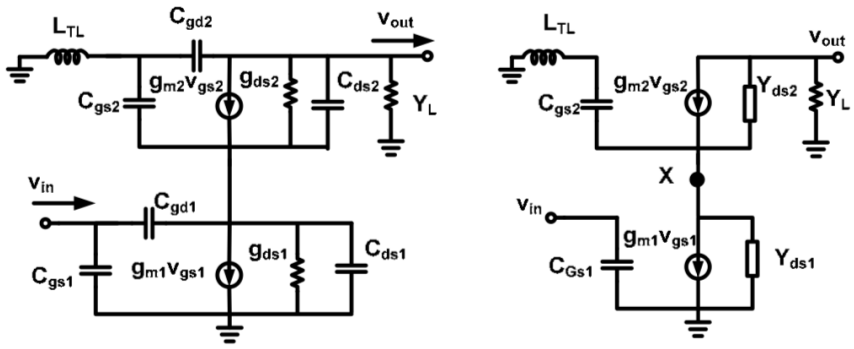


Figure 3·6: Small Signal Model of Cascode Amplifier

Table 3.1 shows the specific value of transistors in the first pre-driver.

Table 3.1: Length and Width of transistors in 1st pre-driver

Parameters	*Values*
Length	120nm
Width Single Finger	5μm
Width All Finger	50μm
Number of Fingers	10
Multiplicity	1
Total Width	50μm

Figure 3·7 shows the schematic of the first pre-driver.

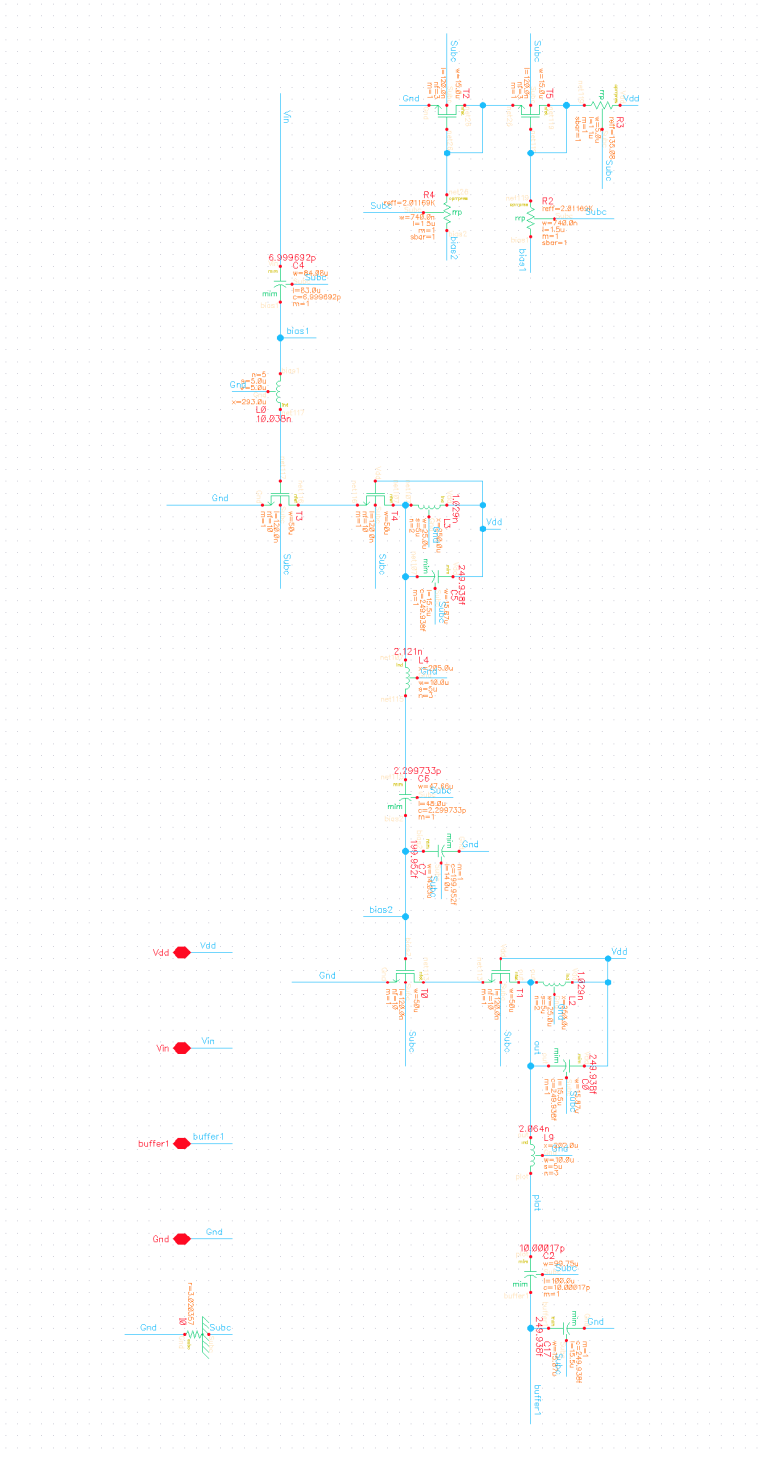


Figure 3·7: First Pre-driver Schematic

3.3.2 Second Pre-driver Design

For the second pre-driver, this work planed to convert the 100mV input signal to 1V output signal. Considering the linearity factor, this thesis chose single common source structure at the first try due to the limited swing of cascode structure. However, it is hard to get 20dB voltage gain through a single amplifier at 10GHz, which can have extremely high power consumption. After several attempts on the second pre-driver, I still chose cascode structure at the end. To get rid of the limitation of output swing, adding a capacitor at the gate of common gate stage, making it ground for AC signal to achieve higher swing. The specific component values of the transistors in the second buffer are shown in Table 3.2 The specific circuit is shown in Figure 3·8

Table 3.2: Length and Width of transistors in 2nd pre-driver

Parameters	*Values*
Length	120nm
Width Single Finger	5μm
Width All Finger	100μm
Number of Fingers	20
Multiplicity	5
Total Width	500μm

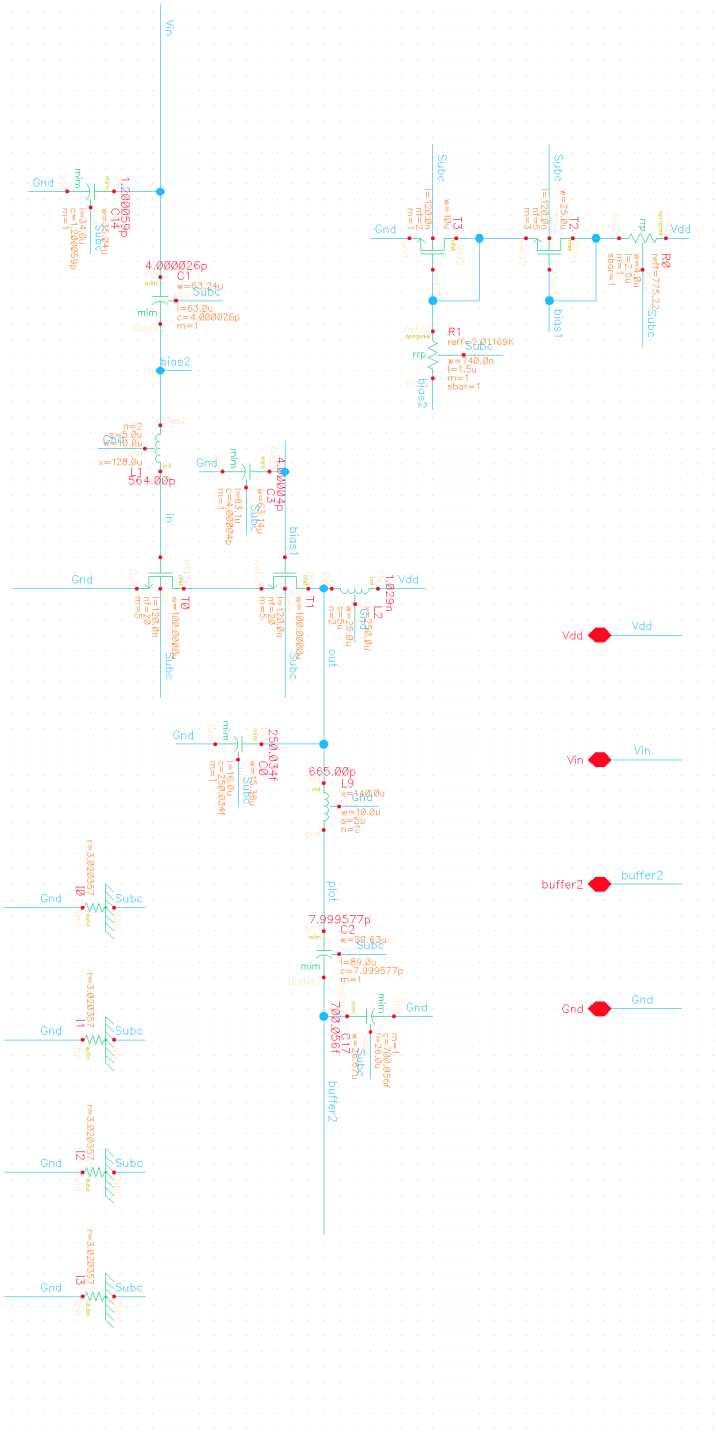


Figure 3·8: Second Pre-driver Schematic

3.3.3 Power Amplifier Design

As mentioned in the last chapter, linear and nonlinear power amplifiers each have their own positives and negatives when it comes to a specific application. As far as this low power design is concerned, output power and power efficiency are the most important performance parameters in choosing an appropriate topology while other parameters, such as power supply consumption, S-parameters, etc., also need to be taken into consideration. Given the fact that the power supply in the future application will be batteries and the power amplifier is the most power hungry RF block in a transceiver, the output power plays a more important role than any other parameter. When choosing a suitable topology among nonlinear power amplifiers, there are many considerations to evaluate. The class AB PA is preferred more than others due to factors presented below. First, class AB power amplifiers are a popular choice for transceiver designs in the research field for applications where output power is important. Second, the class AB power amplifiers have the higher theoretical efficiency and higher output power compared to class A and B. This is a primary reason to choose class AB to see how efficient it can be in reality and how much output power it can provide in terms of this design project.

In order to get 250mW output power on each channel with 50Ω load antenna. Calculating the R_{in}:

$$P_{load} = \frac{{V_p}^2}{2R_L} = \frac{{V_{DD}}^2}{2R_L}, R_{in} = \frac{{V_{DD}}^2}{2P_{load}}$$

assume some losses and choose $R_{in} = 1\Omega$

$$I_{DC} = \frac{2V_{DD}}{\pi R_{im}}, I_{PEAK} = \frac{V_{MAX}}{R_{im}} = \frac{2V_{DD}}{R_{in}}$$

Assuming $V_{GS} = 1.5V$, calculate the required W by using the long channel model.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$$

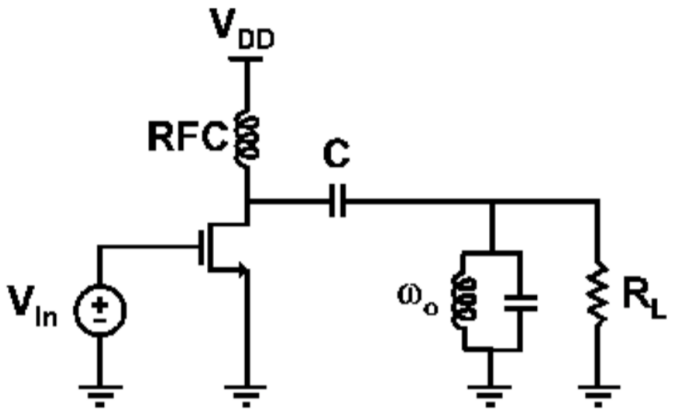


Figure 3·9: Power Amplifier

$$where \mu_n C_{ox} = 0.35 \frac{mA}{V^2}, V_T = 0.35V$$

The specific component values of the transistors in the Power Amplifier are shown in Table 3.3

Table 3.3: Length and Width of transistors in power amplifier

Parameters	*Values*
Length	120nm
Width Single Finger	4μm
Width All Finger	160μm
Number of Fingers	40
Multiplicity	10
Total Width	1600μm

The schematic is shown as Figure 3·10

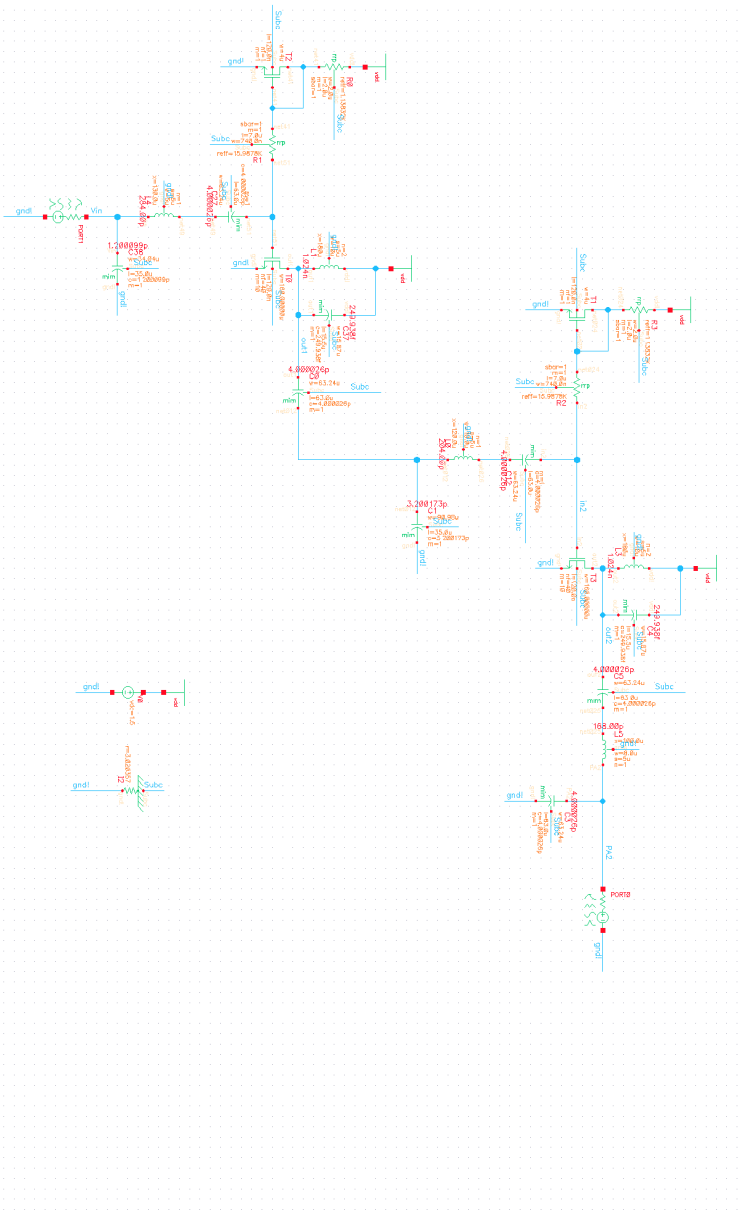


Figure 3·10: Power Amplifier Schematic

3.3.4 Combiner Design

As mentioned before, Wilkinson combiner is a 3-port lossy, matched and reciprocal network as shown in Figure 2·8. However, in this thesis, which is based on 130nm Technology, the traditional Wilkinson combiner cannot be integrated on silicon. Actually, a transmission line has its self-inductance and capacitance per unit length. So the transmission line can be placed by inductors and capacitors which could be integrated on silicon. As Figure 3·11 shown, the transmission line can be replaced by a π circuit. Then we can calculate the impedance of transmission line according to different input impedance and output impedance. $Zin = \frac{{Z_0}^2}{Z_{out}}$ if the output impedance is twice as the input impedance, we can calculate the impedance of transmission line, which is $Z_0 = \sqrt{2}Z_{in}$. When it converts to C-L-C circuit, we can also determine the value of those capacitors and inductors by equation $Z_0 \approx \sqrt{\frac{j\omega L}{j\omega C}}$,$L = \frac{Z_0}{2\pi f}$, $C = \frac{1}{2\pi f Z_0}$.

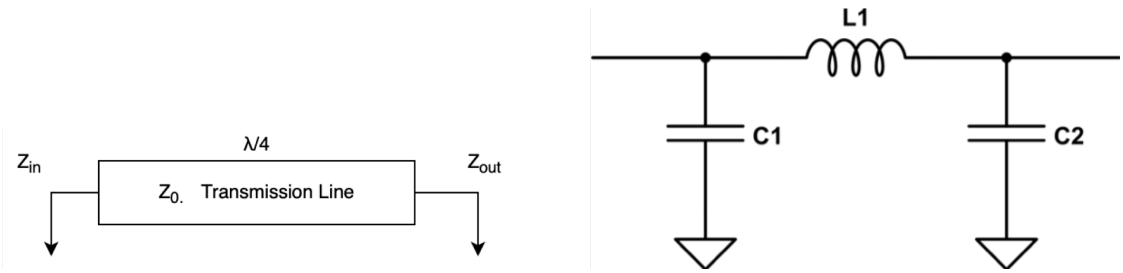


Figure 3·11: (a)Quarter Wavelength Transmission Line (b)Equivalent Lumped C-L-C Circuit

For now, the Wilkinson combiner can also be replaced to an equivalent lumped LC combiner is introduced. The lumped 2×2 combiner/splitter circuit is shown as Figure 3·12. The quarter wave transformer is replaced by an equivalent π(C-L-C) circuit.

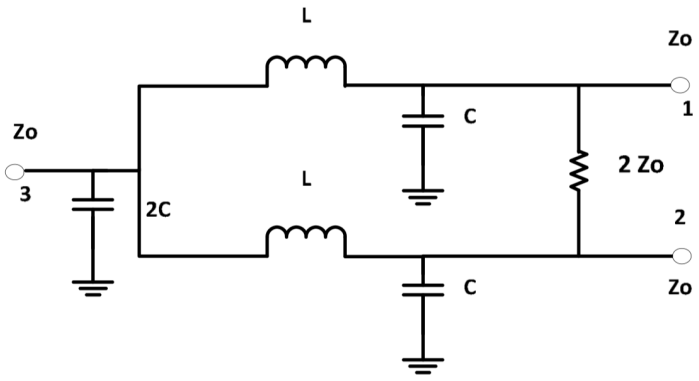


Figure 3·12: Lumped Wilkinson Combiner

$$\omega_0 L = Z_{trans}, L_{trans} = \frac{Z_{trans}}{2\pi f_0}$$

The resonate frequency is defined as $f_0 = \frac{1}{2\pi\sqrt{LC}}$

Based on this 3-port LC network, this thesis presents a lumped LC 4-to-1 combiner, the schematic is shown as Figure 3·13. Here the output impedance is 200Ω, four times as the input impedance, so we can calculate the transmission impedance which is 200Ω, then decide those values of capacitors and inductors at 10GHz.

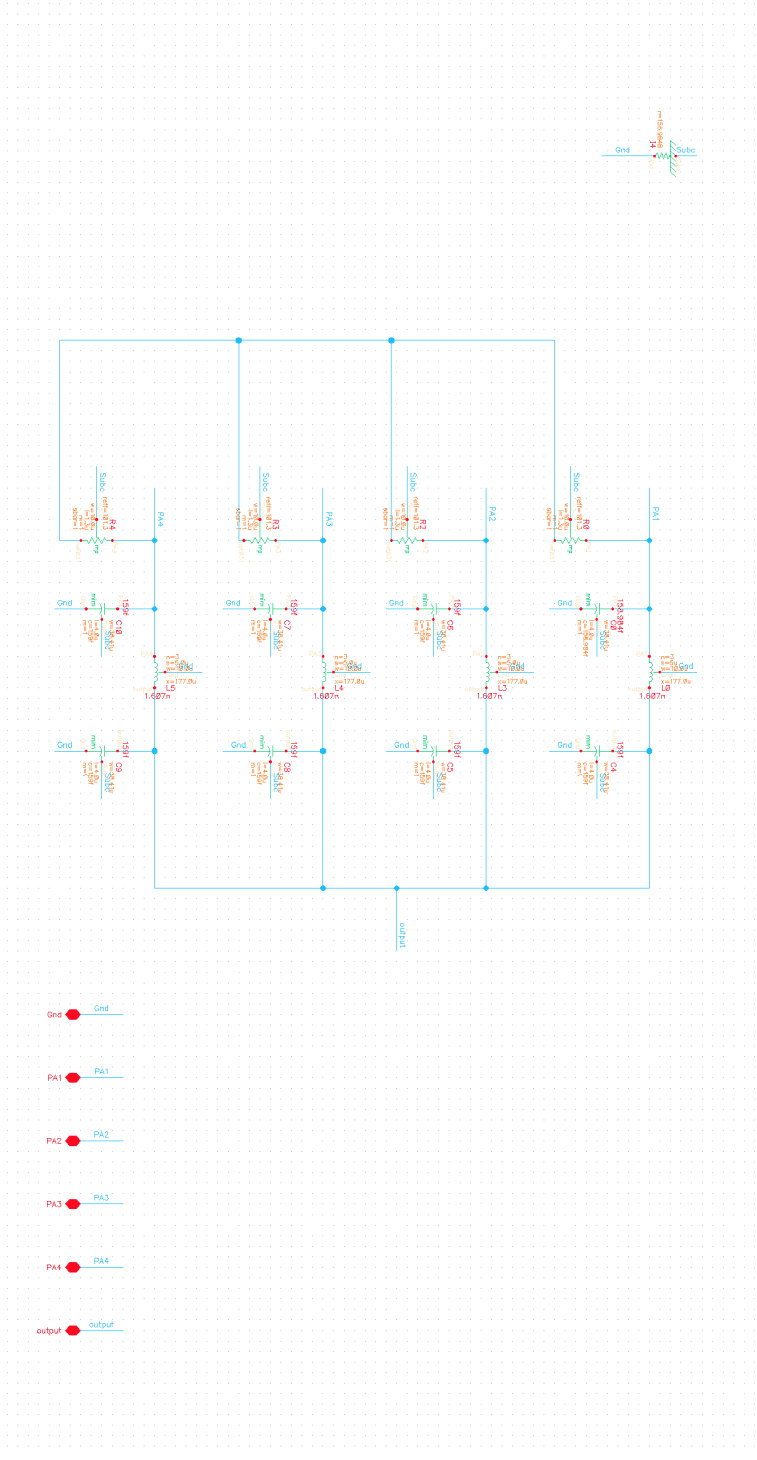


Figure 3·13: Lumped Wilkinson Combiner Schematic

3.3.5 Entire Schematic

After designing each module of my power amplifier, hooking the first pre-driver, the second pre-driver, power amplifier and combiner all together, the whole schematic is shown as Figure 3·14

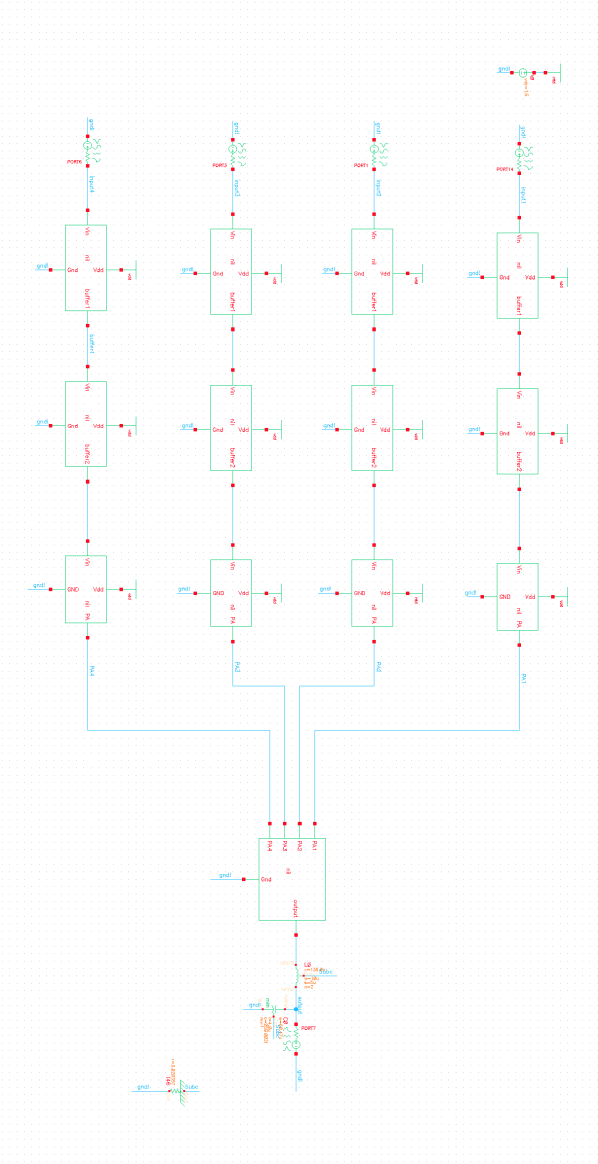


Figure 3·14: The Entire Schematic

Chapter 4

Layout Design

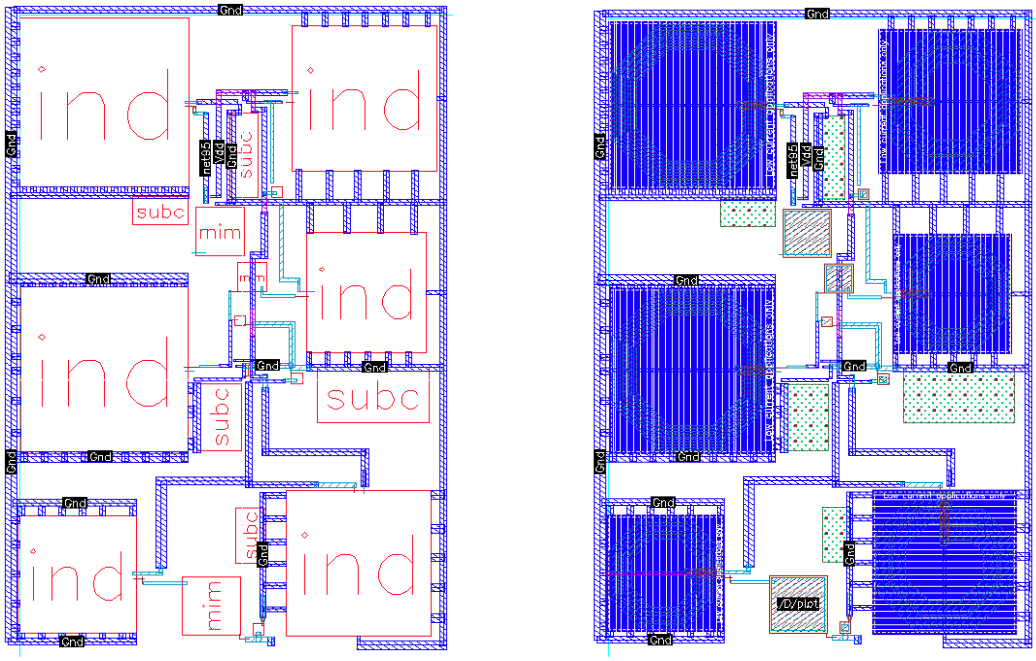
4.1 Overview of Layout Design

4.2 First Pre-driver

Figure 4·1shows the layout design of the first pre-driver. (a)presents overview of the first pre-driver, there are six inductiors in this pre-driver as it utilized two stages of cascode amplifiers. (b)shows the specific components in this module. Figure 4·2shows some details in this layout design, as those transistors are much smaller compared with the inductors and capacitors and can not be seen in the overview version.

4.3 Second Pre-driver

Figure 4·3 shows the layout of second pre-driver. (a)presents overview of the Second pre-driver, there are three inductiors in this pre-driver. (b)shows the specific components in this module. Compared with the first pre-driver, the second pre-driver has less inductors which decreased the area to some degree as it only uses one stage cascode amplifier. Figure 4·4 (a) shows the connection details of transistors. The red one is polysilicon gates of connections; blue one is metal1 layer connections to device drain and source terminals. (b)shows the connections of current mirror bias generator for those transistors. Inductor built on upper layer AM level.



(a) (b)

Figure 4·1: (a)Layout of 1st Pre-driver (b)Specific components in 1st Pre-driver

4.4 Power Amplifier

Figure 4·5 shows the layout of power amplifier. (a)shows the overview of this module, which contains five inductors. (b)shows the specific components used in the power amplifier layout design. Figure 4·6 shows the connection details of the transistors in the power amplifier layout design. The green part in this figure is the Substrate GND connection.

4.5 Combiner

Figure 4·7 shows the layout design of the combiner. (a)presents the overview of the combiner; there are four inductors as this design contains four channels. (b)shows specific components in this module for one of the four channels. Figure 4·8 shows the details in combiner.

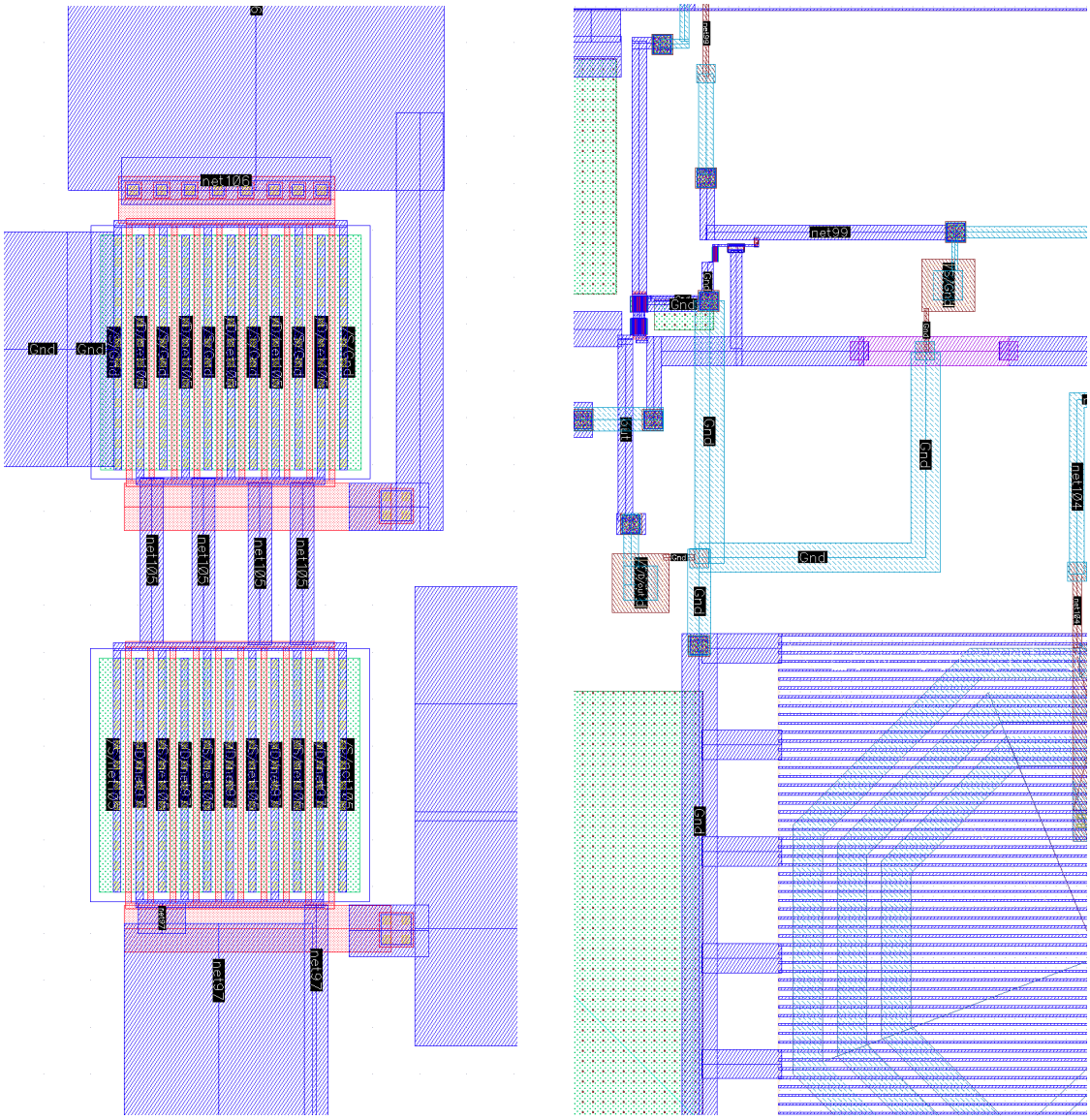
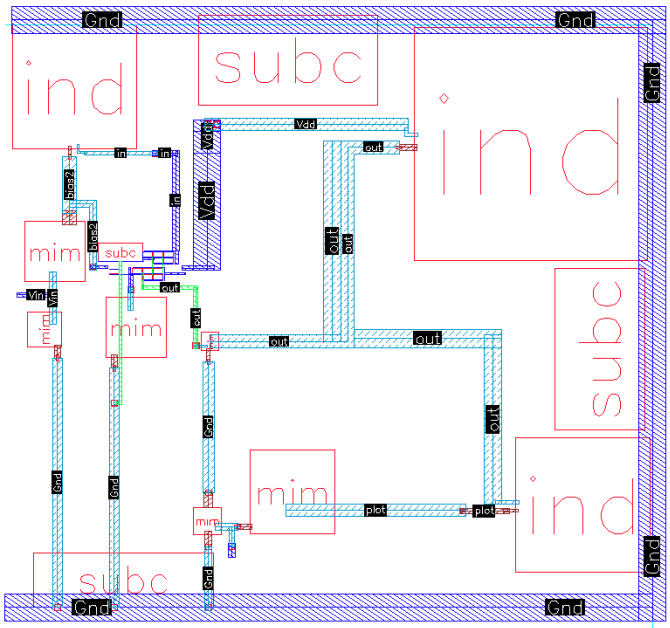
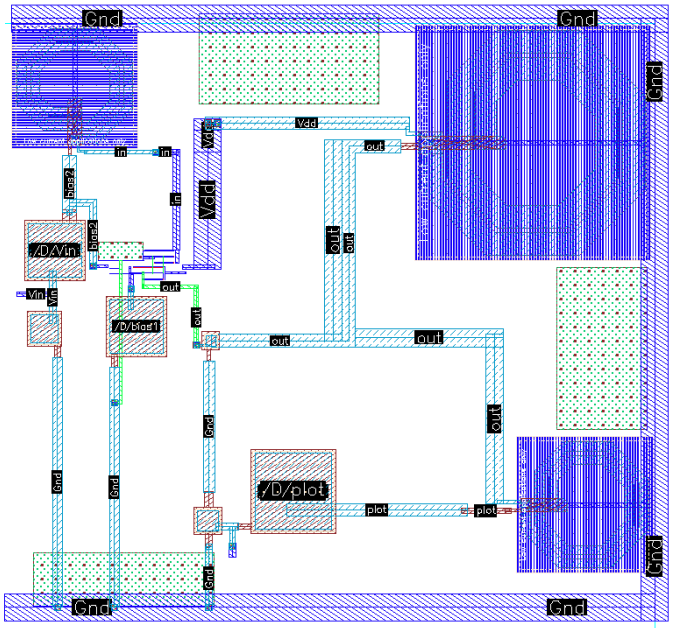


Figure 4·2: (a)Connection of Transistors (b)Connection between different components

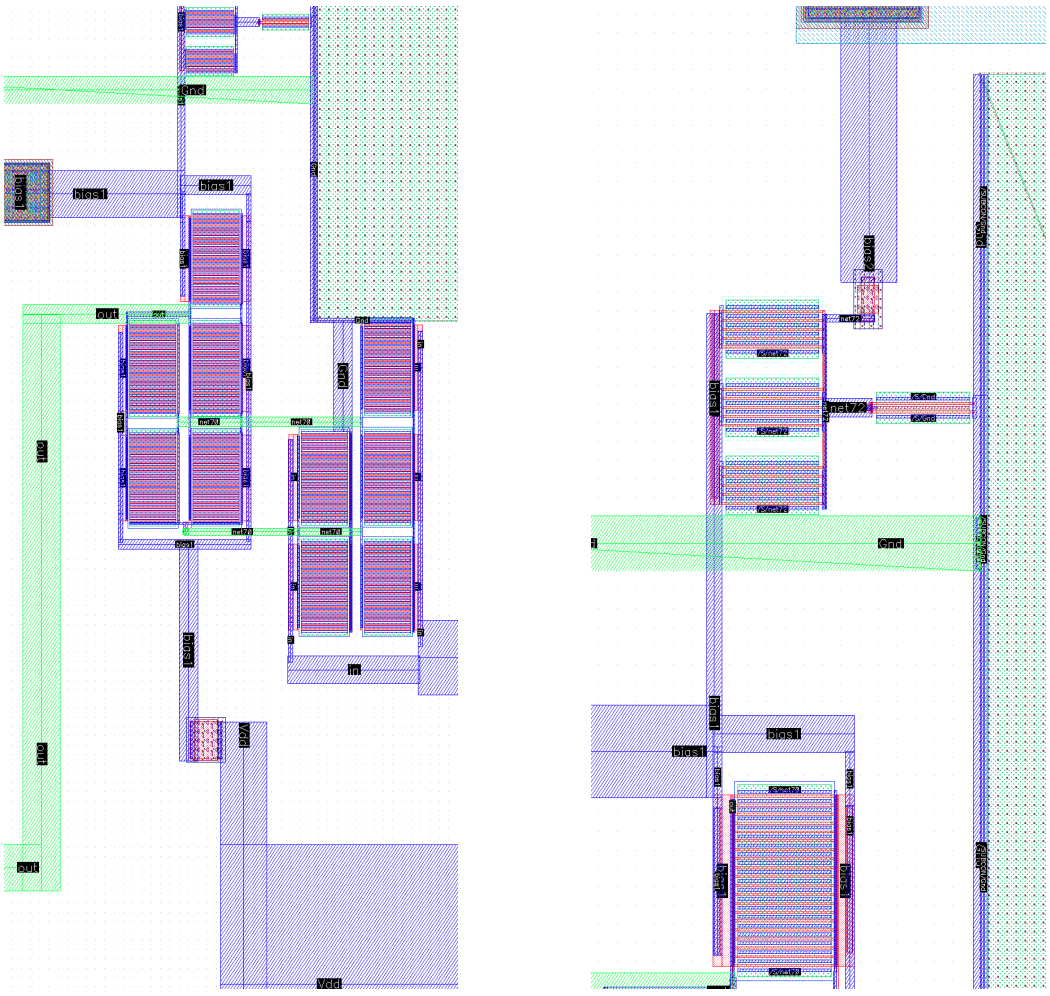


(a)



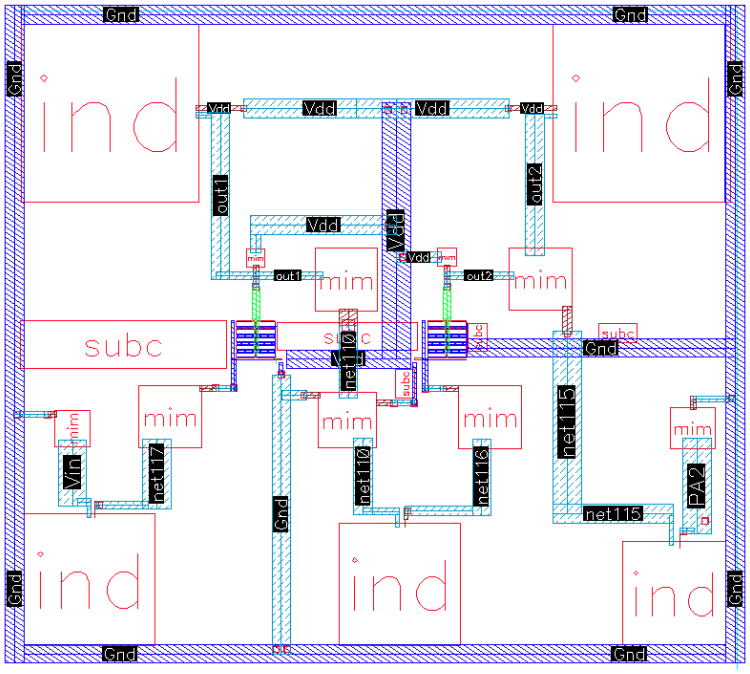
(b)

Figure 4·3: (a)Layout of 2nd Pre-driver (b)Specific components in 2nd Pre-driver

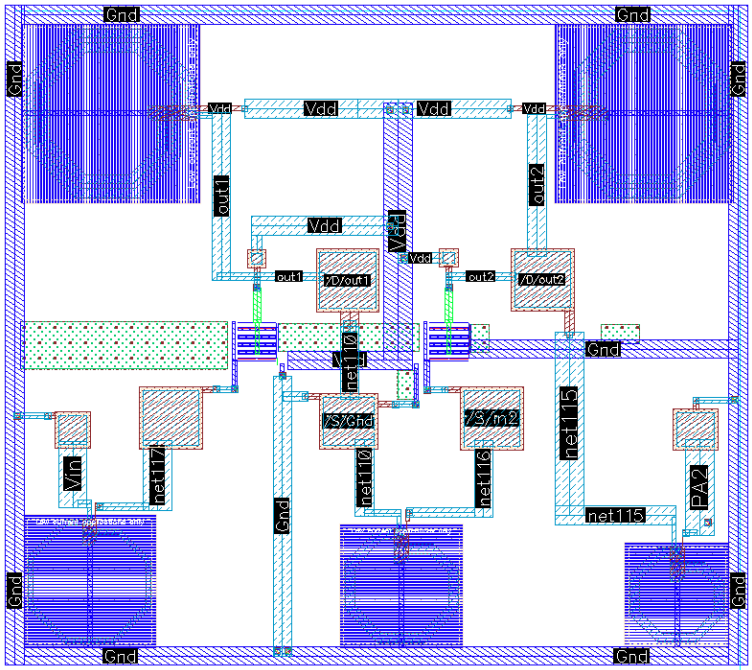


(a) (b)

Figure 4·4: (a)Connection of transisors. (b)Connection for bias generator



(a)



(b)

Figure 4·5: (a)Layout of Power Amplifier (b)Specific components in Power Amplifier

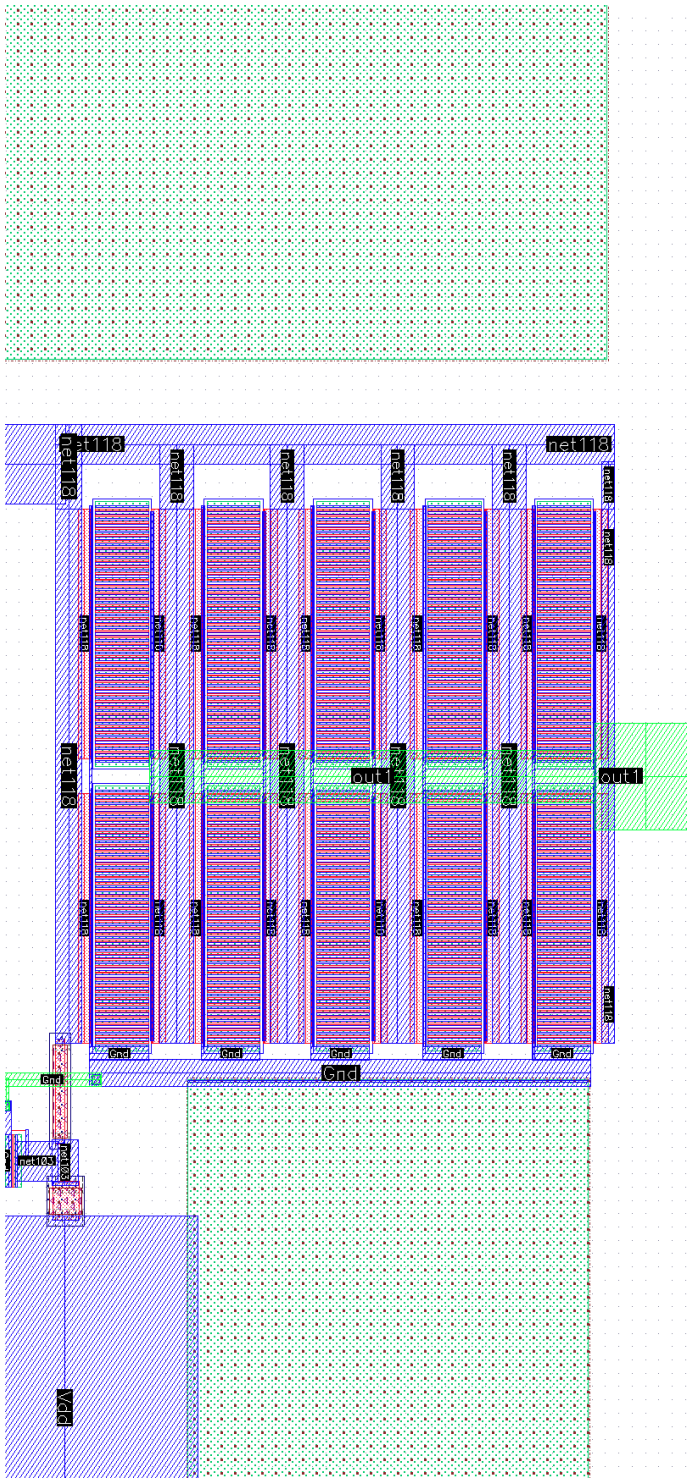
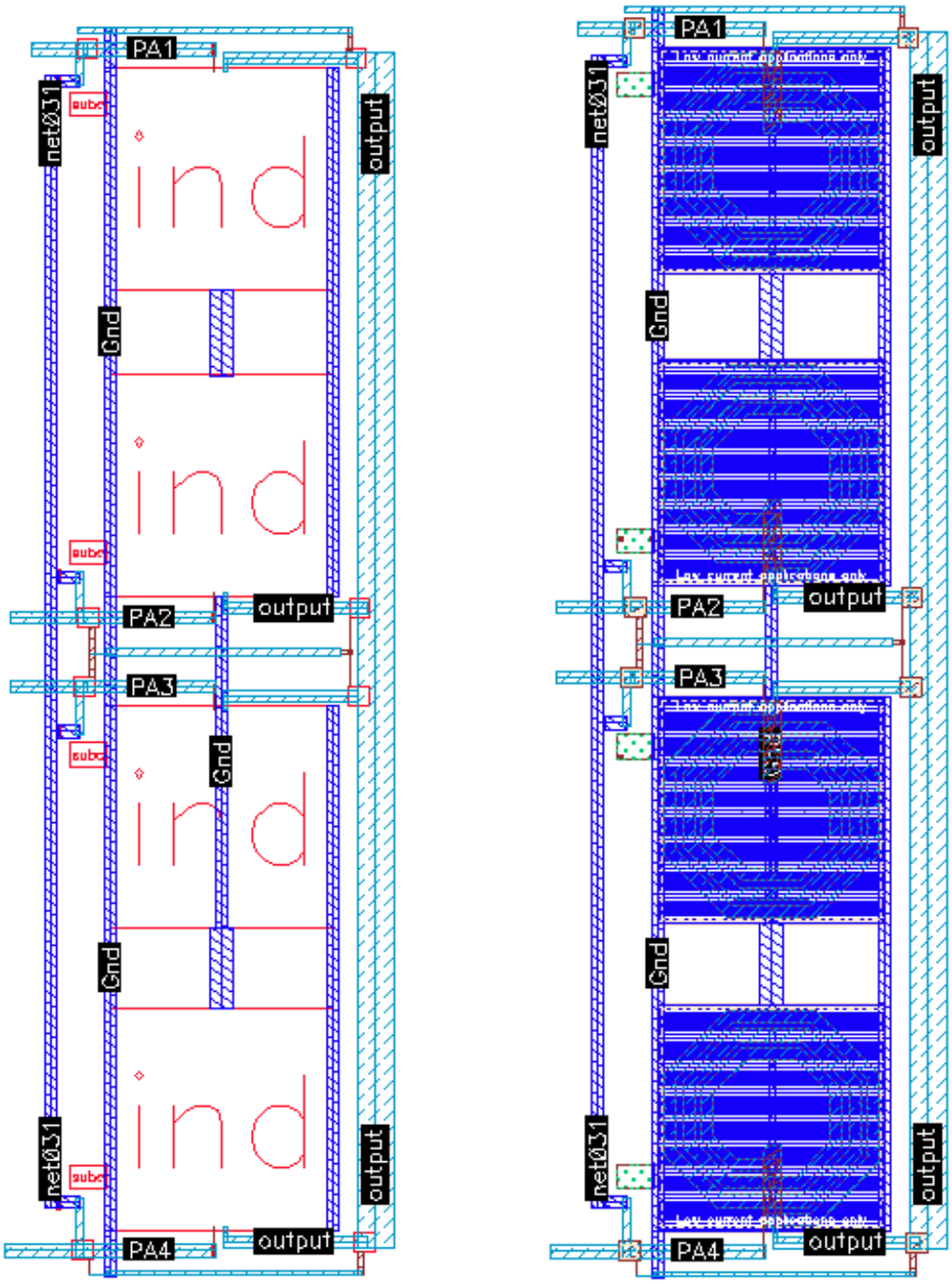


Figure 4·6: Details of Power Amplifier Layout Design



(a) (b)

Figure 4·7: (a)Layout of Combiner (b)Specific components in Combiner

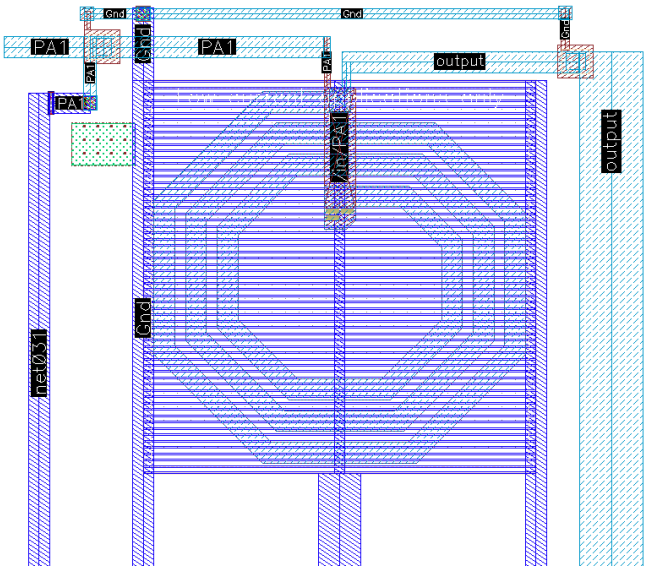


Figure 4·8: Details of a Single Channel in the Combiner Layout Design

Chapter 5

Simulation Results

5.1 Simulation classification

For the simulation part, I introduce several aspects which need to be simulated, these Cadence simulation results are based on schematic-level models using the 130nm Global Foundries 8HP design kit, and then this chapter will give the simulation results of each module in this thesis.

5.1.1 DC Analysis

Running DC simulation usually has two goals, one is to see the DC Operating Bias Points and another is to see the DC power consumption. DC operating point analysis calculates the behavior of a circuit when a DC voltage or current is applied to it. The result of this analysis is generally referred as the bias point, which make sure your transistor is working in the saturation(active) region or any other region designers want. DC analysis will tell designers what would happen if designers simply turned the circuit on and applied no signal to it. By running DC analysis, it can also give an overview of how much power consumption the circuit would require, which helps designers modify the design to meet the requirement of power consumption.

5.1.2 S-parameter

As mentioned in Chapter 2, S-parameter analysis is mainly used for analyzing the stability of the circuit. In cadence S-parameter simulation, the Smith chart is widely used for testing the reflection signals in the input and output port.

5.1.3 AC Analysis

The AC analysis is a small signal analysis in the frequency domain which is to figure out the frequency response of circuit. By running this simulation, designers can see what happens to the circuit when applying well-behaving AC signals into its input, and can see the result of variation in input signal frequency.

5.1.4 Transient Analysis

The transient simulation is the calculation of a networks response to specific input excitations. The results are network quantities (branch currents and node voltages) as a function of time. Substantial for the transient analysis is the consideration of energy storing components, i.e. inductors and capacitors. The relations between current and voltage of ideal capacitors and inductors are given by

$V_C(t) = \frac{1}{C} \int I_C(t) \cdot dt$ and $I_L(t) = \frac{1}{L} \int V_L(t) \cdot dt$

or in terms of differential equations

$I_C(t) = C \cdot \frac{dV_C}{dt}$ and $V_L(t) = L \cdot \frac{dI_L}{dt}$

5.2 First Pre-driver

For the first pre-driver, this design intended to convert a 10mV input RF signal to a 100mV amplitude output signal for the next stage pre-driver. In fact, when utilizing two stages for the first pre-driver, the output voltage becomes twice the planned,

which can achieve 200mV. Figure 5·1 shows the transient simulation result of the first pre-driver. The waveform shows a voltage gain of 25.8dB.

5.3 Second Pre-driver

For the second pre-driver, this design intended to convert 100mV input RF signal from the first pre-driver to 1V output signal for the Power Amplifier module. Figure 5·2 shows the transient simulation result of the second pre-driver. The simulated voltage gain is 19.4dB.

5.4 Power Amplifier

For the power amplifier module, this thesis is supposed to supply a 5V peak output signal, which provides 250mW output power with a 50Ω load. However, due to the linearity factor, the output voltage cannot go as high as this much. Figure 5·3 shows the transient simulation result of this module, the peak voltage is seen to be 4.3V, very close to 5V. Firgure 5·3 shows the simulation result of output power , which is 24dBm.

5.5 Combiner

For the combiner module, it is supposed to combine four 5V input signals to a 10V output signal, as the output power should be four times as one signal channel, then the value of output voltage should be twice that of each channel. Figure 5·4 shows the transient simulation result of this combiner. The losses from this module are not as much as predicted. The simulated output peak voltage is 9.65V with a 5V peak input voltage.

5.6 Entire Design

When combining all module together, there must be some losses between each module due the unperfect matching from the input and output port in each module. Figure 5·5 shows the S-parameter results of the whole design, both of them are below -20dB which means the matching is good as seen from the input and output ports of the whole version. Figure 5·6 shows the transient analysis result, the peak value achieves 7.2V. Figure 5·7 shows the final output power of this thesis. So the final output power is 27.3565dBm, which is 544mW in total.

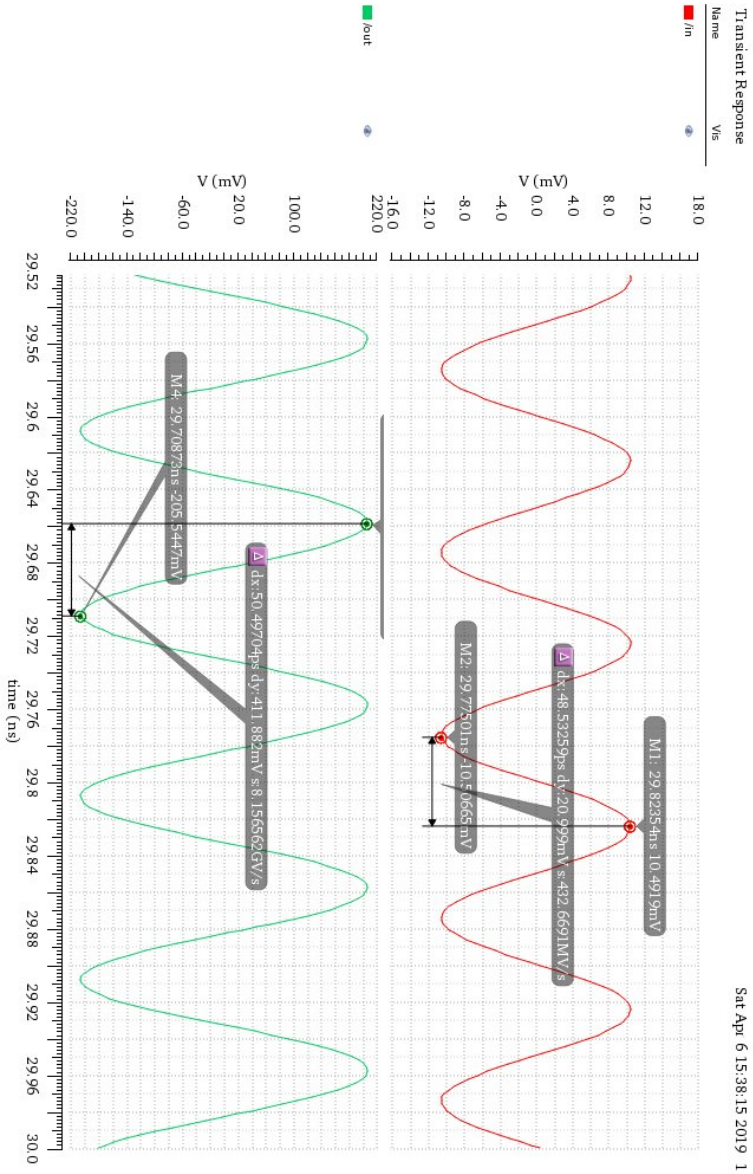


Figure 5·1: Transient Analysis of first pre-driver

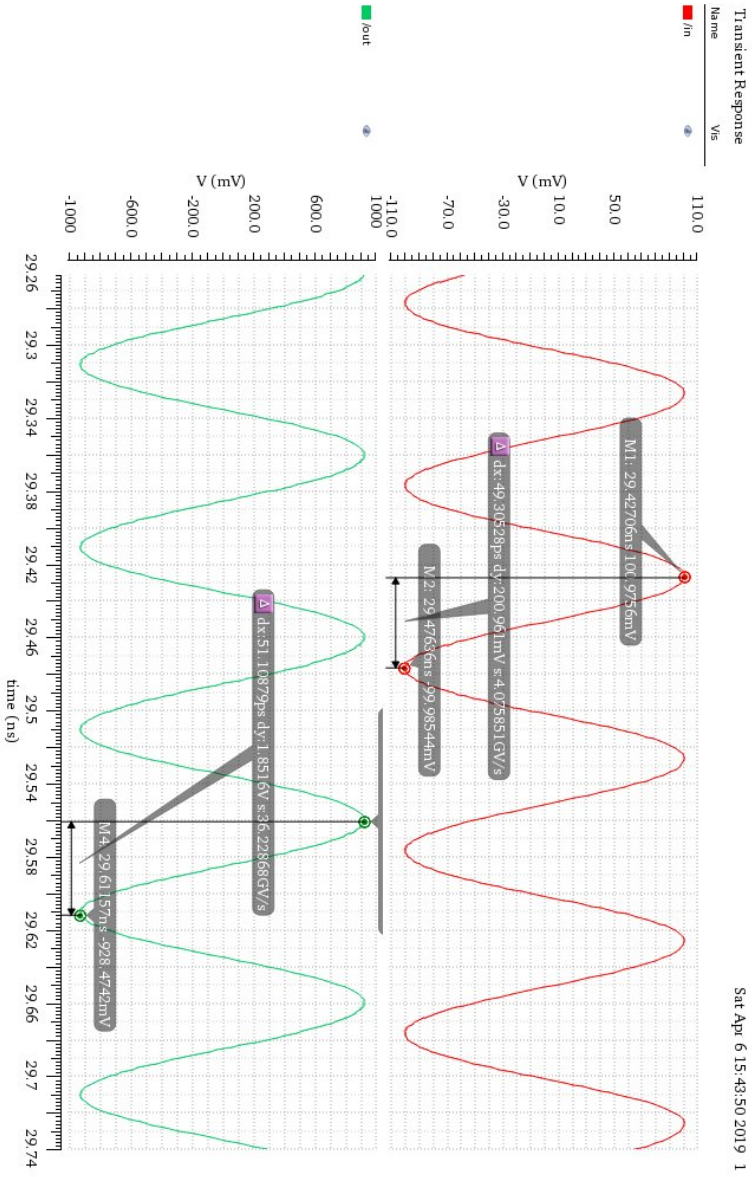


Figure 5·2: Transient Analysis of second pre-driver

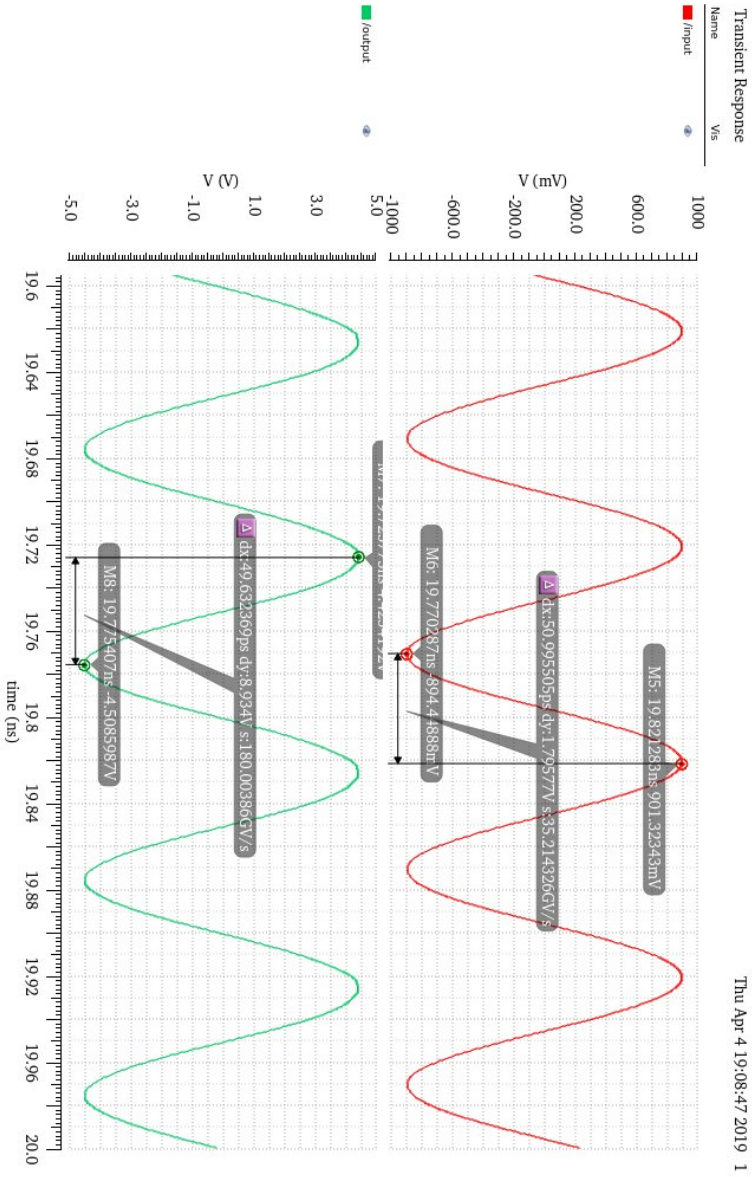


Figure 5·3: Transient Analysis of power amplifier

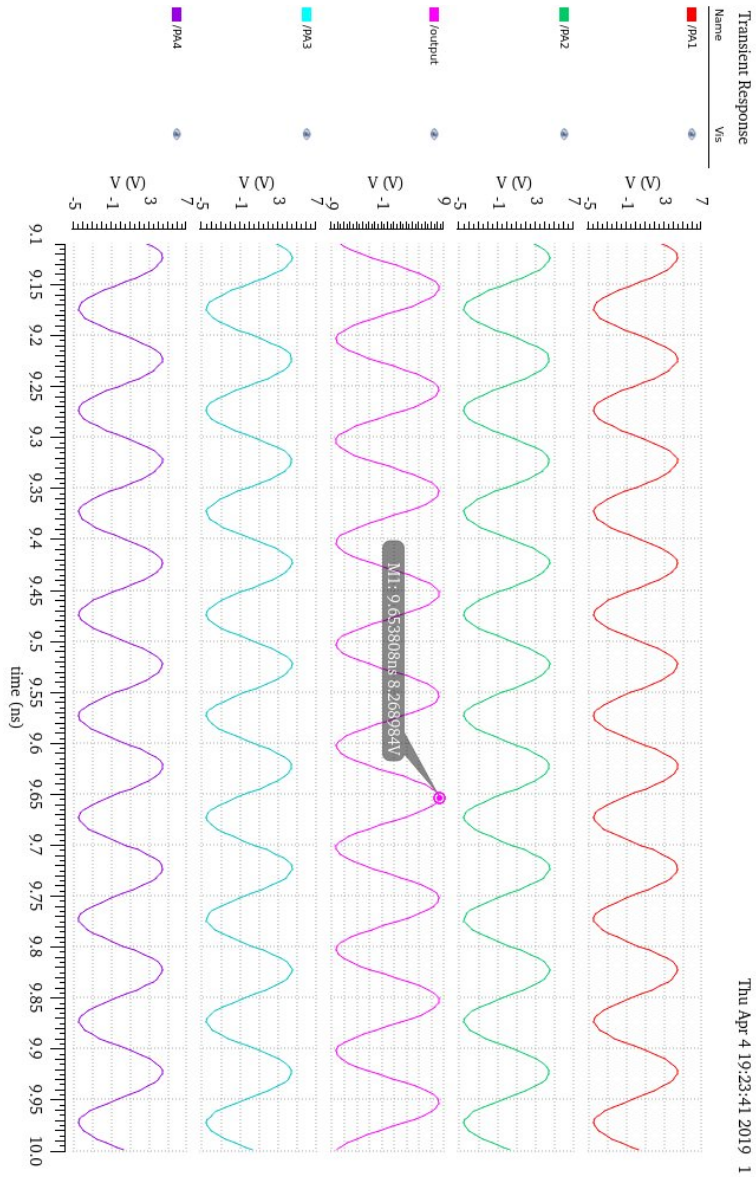


Figure 5·4: Transient Analysis of combiner

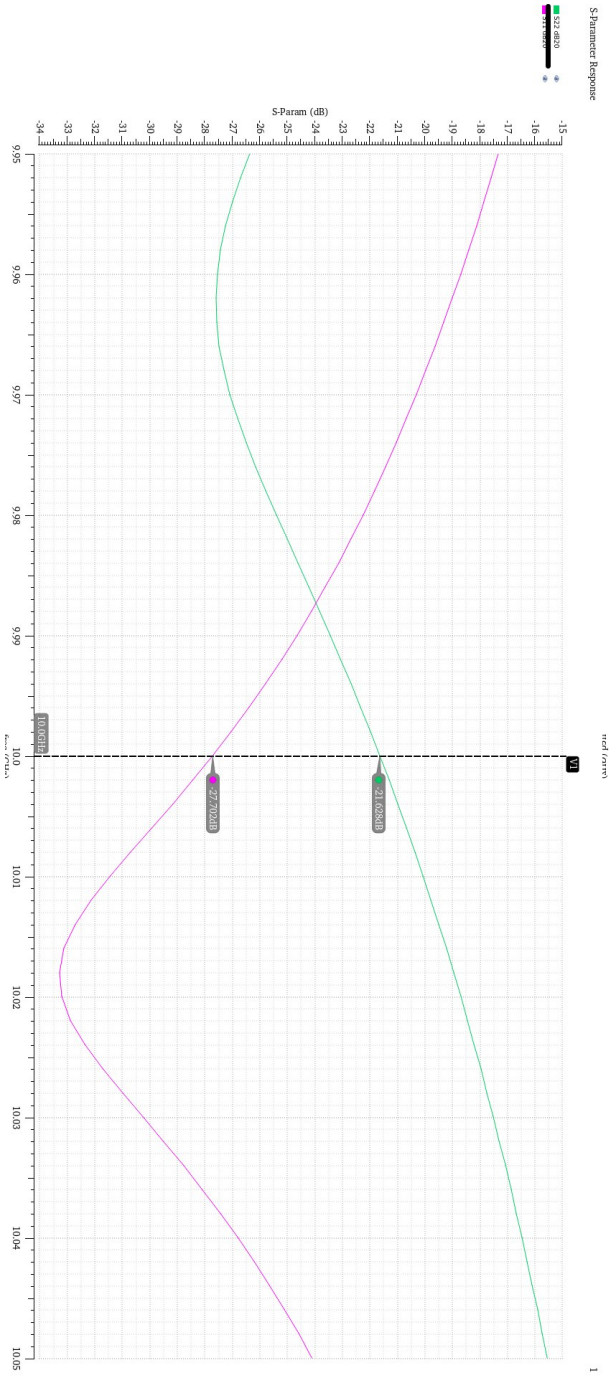


Figure 5·5: S11 and S22 of whole design

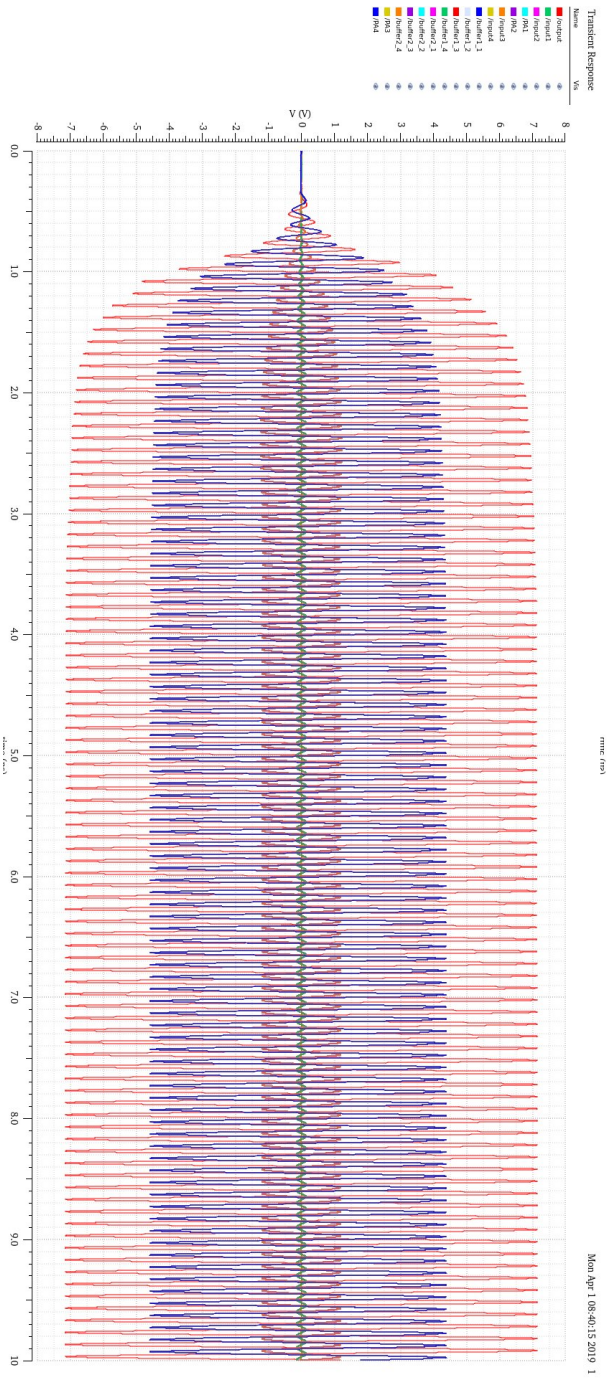


Figure 5·6: Transient Analysis of whole design

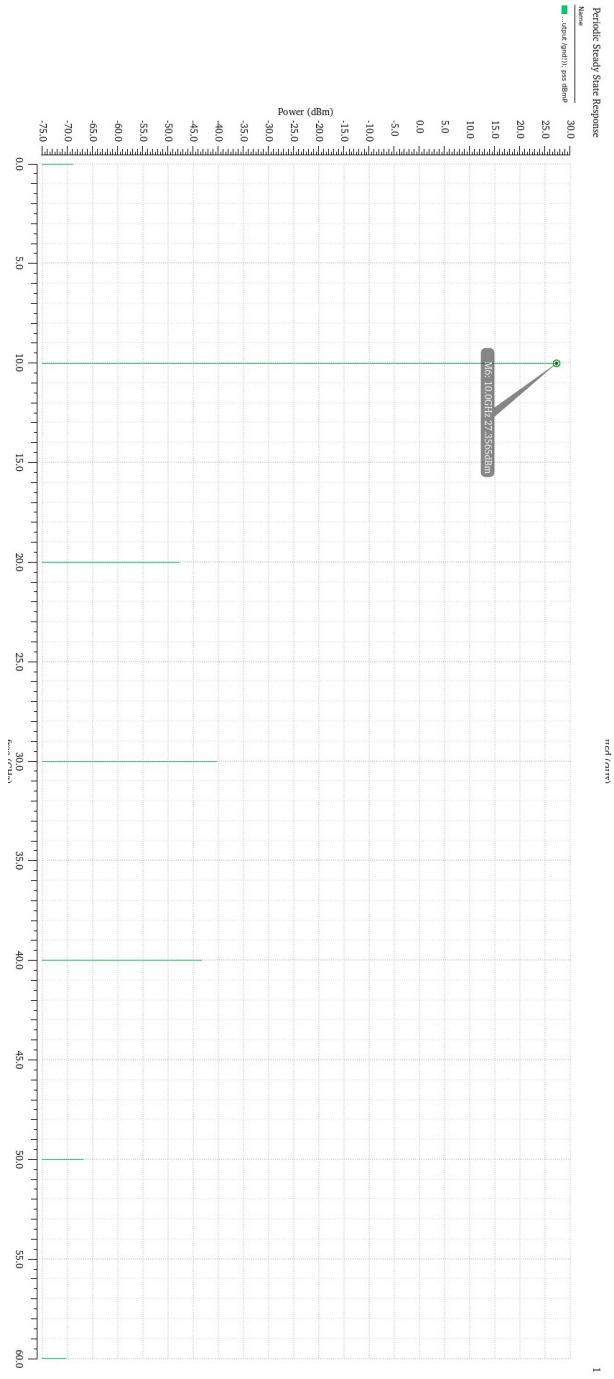


Figure 5·7: Output power of whole design

Chapter 6

Conclusion and Future Work

6.1 Conclusion

Almost every research contributes something to the understanding of the specific subject. Meanwhile, it also opens the door to many other new topics. This work is no exception. To the best knowledge of author, this work is the first one which design a power amplifier by utilizing a 4-to-1 lumped Wilkinson combiner to achieve 27dBm output power at 10GHz with only 1.5V supply voltage based on 130nm CMOS technology with only 783mW DC power consumption from Cadence schematic simulation. Table 6.1 shows some previous work in CMOS power amplifiers design and Table 6.2 shows the conclusion of this work.(Tzschoppe et al., 2014) (Babapour and Javidan, 2015) (Mazzanti et al., 2006) (Madureira et al., 2014) (Ferndahl et al., 2008) (Razavi, 2006) (Love et al., 2017)

Table 6.1: Comparison of previous CMOS power amplifier design

$Frequency$	$OutputPower$	$SupplyVoltage$	$CMOSTechnology$
5.6GHz	22dBm	2.5V	250nm
1.8GHz	30dBm	3.3V	180nm
1.7GHz	23dBm	3V	130nm
2.5GHz	20dBm	2V	130nm
20GHz	10.2dBm	1.5V	130nm
60GHz	6.7dBm	1.5V	90nm
2.5GHz	23.4dBm	5.5V	65nm

Table 6.2: This Work (Based on Cadence Simulation)

$Frequency$	$OutputPower$	$SupplyVoltage$	$CMOSTechnology$
10GHz	27.4dBm	1.5V	130nm

6.2 Future work

Although this work has completed the basic design of power amplifier, it can be improved by decreasing the area and decreasing the power consumption to achieve lower cost and energy efficiency. In order to reduce the area, designer can use inducotr as little as possible. For instance, redesigning the matching part, it is not necessary to match each input and output impedance to 50Ω. Just checking the previous module's output impedance, making the input impedance of next stage the same as previous stage's output impedance. As the first stage pre-driver has two times gain as planed, reducing the bias voltage to a little bit higher than threshold voltage for common source stage to achieve lower power consumption. The same methodology can also be used in second pre-driver and power amplifier. With the development of wireless communication, the power amplifier is still an indispensable part in a RF transceiver. There should be more effort put in to optimize power amplifier module to achieve more efficiency with lower power consumption work to integrate with digital part on the same single chip.

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